Maintenance manual

9919
UHF Frequency Meter

RACAL
The Electronics Group

Racal Instruments Limited Duke Street, Windsor, Berks, England
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LETHAL WARNING

Voltages within this equipment are sufficiently high to endanger life.

Covers are NOT to be removed except by persons qualified and authorised to do so and these persons should always take extreme care once the covers have been removed.

Resuscitation instructions are given overleaf.

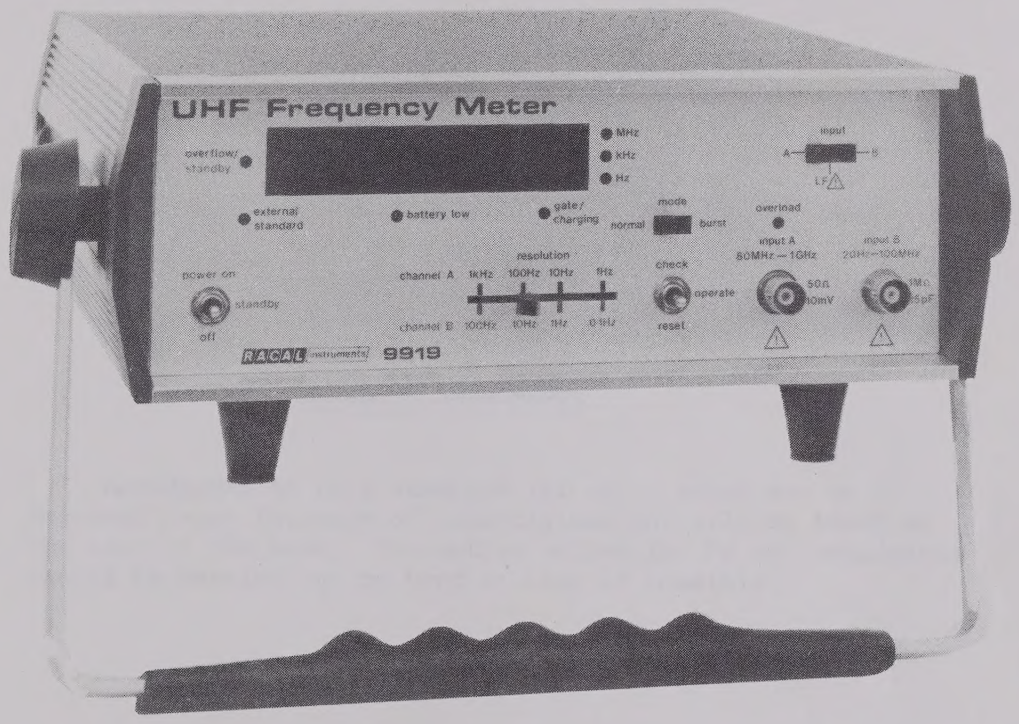
FIRST AID in case of Electric Shock

1. Lay victim on his back.
2. Clear victim's mouth and throat.
3. Tilt victim's head back as far as possible and raise his head.
4. Pinch victim's nostrils.
5. Take a deep breath.
6. Cover the victim's mouth with yours and blow, watching his chest rise.
   Note: Blow forcefully into adults, but gently into children.
7. Move your face away to allow victim to breathe out, watching his chest fall.
8. Repeat first five to ten breaths at a rapid rate; thereafter, take one breath every three to five seconds.
9. Keep victim's head back as far as possible all the time.

Have someone else send for a Doctor

Keep patient warm and loosen his clothing

DO NOT Give liquids
until patient is conscious



RACAL
WOH7135

UHF Frequency Meter 9919

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of indentification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

'POZIDRIV" SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fastners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

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SERIAL-TO-PARALLEL INTERFACE (OPTION 01)

SECTION 1

TECHNICAL SPECIFICATION

TECHNICAL SPECIFICATION

DISPLAY

Format:	Eight, 7 segment LED's. Decimal point positioned automatically.
Latch:	Previous measurement is displayed during period required to complete new measurement. Display is updated automatically at end of each measurement.
Display Time:	Approximately equal to gate time plus 2ms.
Reset:	Manual or automatic A biased Check/Operate/Reset Switch resets the reading to zero when pressed to Reset and released.
Check:	With Check/Operate/Reset Switch in Check position display reads:- Channel A - All digits set to 8 to check all segments. Channel B - Counter reads 1MHz to check operation.
Range Indicators:	Three LED's indicate Hz, kHz, MHz respectively.
Gate/Charging Indicator:	LED illuminated when gate is open or batteries are being charged.
Overflow/Standby Indicator:	LED illuminated on overflow or when standby mode is operating.
Battery Low Indicator:	LED indicates when batteries require charging.
Overload Indicator:	LED indicates when 'A' channel input exceeds approximately 7V r.m.s.
External Standard Indicator:	LED indicates when external standard is in use.

INPUT 'A'

Frequency Range:	80MHz to 1100MHz.
Sensitivity:	Better than 10mV up to 1GHz. Better than 50mV up to 1.1GHz.
Signal Range:	10mV to 5V r.m.s. with automatic gain control.
Input Impedance:	50Ω (nominal) BNC connector.
Damage Overload:	10V r.m.s.
Automatic Gain Control:	50dB minimum range. AGC output is available at two pins on rear panel.

INPUT 'B'

Frequency Range:	20Hz to 100MHz.
Sensitivity:	Better than 10mV up to 80MHz. Better than 50mV up to 100MHz.
Input Impedance:	1MΩ in parallel with 25pF.
Maximum Input Levels (Damage Overload Levels):	250V r.m.s. up to 10kHz. 50V r.m.s. up to 100kHz. 10V r.m.s. above 100kHz. 400 volts d.c.
Automatic Gain Control:	Approximately 50dB range. A clipping circuit becomes effective above 10V peak-to-peak.

FREQUENCY MEASUREMENT

Range:	Channel 'A' 80MHz to 1100MHz (pre-scaled by 20). Channel 'B' 20Hz to 100MHz (pre-scaled by 2).
Accuracy:	± 1 count ± frequency standard accuracy.
Gate Times:	0.02s, 0.2s, 2.0s, 20s.

FREQUENCY MEASUREMENT (Cont'd)

Resolution:	Channel 'A': - 1kHz, 100Hz, 10Hz, 1Hz. Channel 'B': - 100Hz, 10Hz, 1Hz, 0.1Hz.
Burst Mode:	In the Burst Mode the gate remains closed until triggered by incoming signal. After measurement the display is held until manually reset. The minimum signal duration is 40ms plus gate time.
LF Multiplier:	See Option 09.

FREQUENCY STANDARD 04A

Type:	Model 9442. A fast warm-up ovened oscillator suitable for the vast majority of applications and normally fitted unless otherwise requested.
Frequency:	5MHz.
Ageing Rate:	± 3 parts in 10^9/day after 3 months continuous.
Warm-up Time:	Better than ± 2 parts in 10^7 within 6 minutes.
Temperature Stability:	Better than ± 3 parts in 10^9 per °C over the range -10°C to +45°C.

FREQUENCY STANDARD 04B

Type:	Model 9421. An ovened oscillator of the utmost precision for use when the highest long term accuracy is essential.
Frequency:	5MHz.
Ageing Rate:	± 5 parts in 10^{10}/day after 3 months continuous operation.
Warm-up Time:	Better than ± 1 part in 10^7 within 20 minutes.
Temperature Stability:	Better than ± 6 parts in 10^{10} per °C over the range -10°C to +45°C.

FREQUENCY STANDARD 04C

Type:	An unovened crystal oscillator suitable for non-critical applications or where the instrument will normally be used with the customer's external standard.
Frequency:	5MHz.
Ageing Rate:	± 1 part in 10^6 per month.
Temperature:	± 8 parts in 10^6 over temperature range 0°C to +55°C. ± 3 parts in 10^6 over temperature range +20°C to +40°C.

STANDARD FREQUENCY OUTPUT

Frequency:	1MHz.
Level:	Standard t.t.l. output.
Waveform:	Approximately rectangular.
Connector:	BNC socket on rear panel.

EXTERNAL STANDARD INPUT

Frequency:	1MHz.
Minimum Level:	500mV r.m.s.
Maximum Level:	10V r.m.s. 400V d.c.
Input Impedance:	Approximately 200Ω (a.c. coupled).
Connector:	BNC socket on rear panel. The instrument automatically changes to external standard when standard input is connected.

REMOTE CONTROL

Local/Remote Selection:	Control signal applied to rear panel 28 way connector overrides front panel controls. (see page Tech. Spec. (10) para. A4).

REMOTE CONTROL (Cont'd)

Functions Programmable:	Timebase, Input Channel and Frequency Multiplier (option). External Hold and External Reset.
Control Inputs:	Standard t.t.l. logic levels.

DATA OUTPUTS

Display:	Serial BCD output is provided at standard t.t.l. logic levels giving 8 digits and decimal points.
Function and Control:	Static timebase and overflow outputs with timing controls are provided.

POWER REQUIREMENTS

Supply:	94V to 132V or 188V to 265V r.m.s., 45 to 450Hz a.c. or optional battery pack.
Voltage Ranges (a.c.):	Eight ranges selected by transformer connection and link:-

94V to 106V	200V to 225V
106V to 119V	212V to 239V
118V to 132V	223V to 251V
188V to 212V	235V to 265V

Consumption:	20VA approximately.

ENVIRONMENTAL CONDITIONS

Operating Temperature Range:	0° to $+55^{\circ}$C (0°C to $+40^{\circ}$C with Option 07)
Storage Temperature Range:	-40°C to $+70^{\circ}$C (-40°C to $+60^{\circ}$C with Option 07)
Humidity:	95% r.h. at $+40^{\circ}$C.
Environmental Specification:	Tested in accordance with IEC 68 (BS 2011) recommendations.
Safety Standard	Designed to meet IEC 348 (BS 47 43) recommendations.

MECHANICAL

Dimensions:	Height: 83 mm (case only) 110 mm overall Width: 240 mm (case only) 284 mm overall Depth: 268 mm
Weight:	Approximately 2.7 kg excluding battery pack Battery pack 1.5 kg.
Accessories Supplied:	Operators Manual, Spare Fuses and Supply Voltage Label.

OPTION 01: SERIAL TO PARALLEL INTERFACE

Data and Control Information:	This unit provides an interface between the 28-way data output of the 9919 and a 50-way connector to a printer, or remote display. It converts the serial b.c.d. data to parallel format and transfers the following information. 8 decades of data in 4 line BCD weighted 1248, 3 line decimal point position, print command, print hold, reset, overflow and time-base information. All logic levels t.t.l. compatible.

OPTION 04: ALTERNATIVE FREQUENCY STANDARDS

Refer to pages Tech.Spec.(3) and (4).

OPTION 07 BATTERY POWER PACK

Mechanical:	Battery Pack is mounted on a metal tray inside the instrument and connected via a polarised 4-pin connector.
Selection:	By means of 3-position Mains/Charge/Battery switch on rear panel.

OPTION 07 (Cont'd)

Battery Life:	$3\frac{1}{2}$ hours minimum continuous at +20°C, 15 hours minimum on standby at +20°C.
Battery Condition:	Indicated by 'Battery Low' lamp on front panel.
Charge Time:	14 hours at +20°C.
Standby Facility:	With power switch in standby position only the internal standard is operational. Pressing the Reset Switch activates the Counter for approximately $1\frac{1}{2}$ minutes, after which it reverts to the standby condition.

OPTION 09 FREQUENCY MULTIPLIER

Function:	To increase measurement resolution at low frequencies on 'B' input channel.
Frequency Range:	20Hz to 5kHz.
Multiplication:	x 100.
Gate Time:	Fixed at 2s.
Resolution:	0.01Hz.

OPTIONAL ACCESSORIES

(1) 19-inch Rock Mounting Kit (Part No. 11 - 1126).

(2) Solid Carrying Case for portable use (Part No. 15-0450).

(3) Padded Carrying Case (part No.15-0444)

(4) Adaptor for connecting to rear panel 28-way Data Output edge connector (Part No. 23-5147).

SUPPLEMENTARY DATA

INPUT/OUTPUT CONNECTIONS

A1 Data and Command information is available via a 28-way edge connector accessible by removing a cover on the rear panel. The facilities and pin connections are listed in Table 1 below. The logic for the time base and channel selection codes is given in Tables 2 and 3, together with supplementary information.

TABLE 1

Input/Output Connector

Pin	Facility		Pin	Facility	
	Data Output	Remote Input		Data Output	Remote Input
1	-5.2V	-	A	0V	-
2	+5V	-	B	$\overline{\text{Overflow}}$	-
3	Key Way	-	C	Key Way	-
4	$\overline{4}$ (BCD)	-	D	$\overline{1}$ (BCD)	-
5	$\overline{8}$ (BCD)	-	E	$\overline{2}$ (BCD)	-
6	-	$\overline{\text{External Hold}}$	F	5kHz sync.	-
7	-	$\overline{\text{External Reset}}$	H	$\overline{\text{Main Gate}}$	-
8	-	-	J	-	-
9	$\overline{c}$ Function	-	K	$\overline{z}$ Time Base	$\overline{z}$ Time Base
10	$\overline{b}$ Information	-	L	$\overline{y}$ Information	$\overline{y}$ select
11	$\overline{a}$	-	M	$\overline{x}$ (Table 2)	$\overline{x}$ (Table 2)
12	$\overline{\text{Ro}}$	-	N	-	$\overline{\text{LF Select}}$
13	$\overline{\text{Hold/Reset}}$	-	P	-	-
14	Channel	Channel Select	R	-	Remote Select

NOTE:

(1) For information on External Hold and Reset inputs, and Remote Control, refer to page Tech.Spec.(9).

(2) The overflow level on pin B is a static indication.

NOTES ON TABLE 1

TIME BASE CONTROL

A2 The required gate times (resolution) are selected by a three line code x-y-z which controls the time base in the CD1 chip.

Table 2 gives the logic code at the Data Output edge connector, on pins M, L and K. The opposite logic is applied to the CD1 chip itself.

TABLE 2

Time Base Selection Code

Code and Pin Reference x	y	z	Gate Time (seconds)
M	L	K	
0	1	1	.02
1	0	1	0.2
0	0	1	2
1	1	0	20

FUNCTION AND CHANNEL CODES

A3 The 9919 is a single function instrument, therefore data connector pins 9, 10 and 11 are held at logic '1'. The code for remote channel selection is given in Table 3.

TABLE 3

Channel Selection Codes

Data Connector Pin 14	Channel Information and Selection
'1' (or open circuit)	Channel 'B'
'0'	Channel 'A'

Remote Select Line

A4 To permit remote selection of time base (gate time) and input channel the remote selection line (Table 1, pin R) must be held at logic '0'. This allows the remote channel and gate time selection to override the local front panel controls, provided that the Input switch is not in the LF position.

External Hold

A5 If, when used with external circuitry, it is required to extend the cycle time, the external hold, (logic '0', pin 6) must be applied within the gate time or up to 200μs after gate closure. In order to initiate a new cycle of measurement, the external hold must go 'high' for not less than 400μs.

External Reset

A6 External reset is achieved by the application of logic '0' to pin 7 of the connector for a period of not less than 200ns. On returning to '1' level this will reset the display to 'all zeros' and initiate a new measurement cycle.

LF Select

A7 External selection of the LF mode is achieved by the application of logic '0' to pin N, this overrides the switches on the front panel (LF mode is operative only when Input 'B' is in use).

Settling Time

A8 When changing input channels on remote control, allow a short amplifier settling time before taking a new reading. This should be especially borne in mind when on automatic operation.

SECTION 2

DESCRIPTION

OPERATION AND MAINTENANCE

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1.1 The 9919 is an eight digit frequency meter with a measurement capability up to 1100MHz and containing a number of advanced operational features. The instrument operates from a.c. mains supplies and contains a battery charging facility. An internally-fitted battery pack is available as an option.

1.2 Four gate times of .02, 0.2, 2 and 20 seconds are provided. The switch is annotated with the resolution of the input. The frequency units of the display are indicated by the associated MHz, kHz and Hz l.e.d. indicator lamps. A GATE lamp illuminates when measurement is in progress. An OVERFLOW/STANDBY lamp illuminates if the 'A' Channel display is over-filled (the reading would exceed 'all nines'), or if the unit is in standby mode. The display and all indicator lamps are l.e.d's (light-emitting diodes) with provision for 'segment check' on the display.

INPUTS

1.3 Two input channels are provided: Input 'B' is a high impedance (1MΩ) channel covering the range 20Hz to 100MHz, prescaled by two, with a a.g.c. Input 'A' is a 50Ω channel covering the range 80MHz to 1100MHz, prescaled by 20, with a.g.c. and overload indicator.

SPECIAL FACILITIES

'Burst' Measurement

1.4 This facility is provided for measurements on signals which occur in short bursts at irregular intervals. The minimum burst duration is 40ms plus gate time. By selecting BURST and depressing the RESET switch, the display (except the decimal point) is rendered blank until a burst of signals occurs. The instrument then indicates all zeros, measures and displays the frequency of the signal burst, and holds the display until manually reset.

Battery Economy (Standby) Facility

1.5 When the optional battery pack is fitted and continuous readout is not required, a significant increase in battery operating time can be obtained by switching to STANDBY. The instrument is then 'off' except for the internal frequency standard. If the RESET switch is depressed the instrument will operate normally for approximately one and a half minutes after which it reverts to the standby condition. This operation may be repeated as required. Although it is intended for battery economy purposes, the same operation may be used on STANDBY mode with a.c. power supply, if desired.

LF Multiplier (Option)

1.6 An optional 'LF' facility is suitable for easier measurements of low frequencies such as audio tones. By means of a frequency multiplication technique the resolution below 5kHz is improved by a factor of 100 with a measurement time of two seconds. The Burst facility is not operative in LF mode.

AGC Output

1.7 The 'A' Channel amplifier automatic gain control voltage is brought out to two pins on the rear panel (AGC O/P) for use as a peak indication in, for example, transmitter tuning.

Remote Control

1.8 Remote control of the time base channel selection and of the LF Multiplier is available using TTL levels via the 28-way connector at the rear of the unit, see Table 1 on page Tech.Spec.(8).

Segment and Counter Check

1.9 By selecting INPUT 'A' and CHECK, the readout will display 'all 8's', thus checking that the segments in the display LED's are functioning correctly. By selecting INPUT 'B' and CHECK, the instrument will measure and display the internal 1MHz reference frequency.

FREQUENCY STANDARD

1.10 Customers are offered a choice of two high stability temperature controlled frequency standards from the Racal range, or an unovened oscillator. Details are given on pages Tech.Spec.(3) and (4). The high stability units should be serviced only by Racal Instruments, or authorised agent. An aperture in the rear panel provides access for calibration of the frequency standard.

1.11 A 1MHz reference frequency, derived from the standard in use, is available from a BNC socket on the rear panel. An external frequency standard can be connected via a rear panel BNC socket. When this facility is in use the EXTERNAL STANDARD indicator on the front panel is illuminated.

POWER SUPPLY

AC (Mains) Supply

1.12 The instrument operates from a.c. supplies of 94 to 132V and 188 to 265V, 45 to 450Hz. A tapping on the internal mains transformer must be correctly set according to the user's supply voltage. A label fixed to the rear panel should indicate the selected range. Spare labels are supplied with the instrument for voltage ranges other than 223 to 251V.

Battery Power Supply (Option)

1.13 The instrument can operate either from normal a.c. mains supplies, or from an internal battery pack containing re-chargeable nickel cadmium cells. The batteries allow up to 4 hours continuous operation from the full charged condition. A 3-position rear panel switch selects mains or battery power, or full-rate charging of the batteries from the internal charging circuit. When on battery operation a warning light indicates when battery voltage is low.

Battery Charging

1.14 To fully charge a discharged battery requires 14 hours. Avoid overcharging as it will progressively reduce battery charge capacity. When the instrument is operating from a.c. mains supply the batteries receive a trickle charge which can continue indefinitely without detriment to the batteries.

MAINTENANCE

1.15 The customer is recommended to take advantage of the servicing facilities offered by Racal Instruments Ltd., and agents.

CARRYING HANDLE

1.16 The instrument is fitted with a combined carrying handle and bench stand. To adjust the stand, press in the two handle bosses simultaneously, while setting the stand to the desired position.

OPTIONS

1.17 The various options available are summarized on pages Tech Spec. (5) and (6). The frequency multiplier option is described in Chapter 4 and a circuit diagram (Fig. 6) is given in Section 3 of the manual. The functions and use of the Serial-to-Parallel Interface Unit are fully described in an Appendix in Section 4.

DESCRIPTION OF CONTROLS AND CONNECTIONS

POWER ON/OFF and STANDBY Switch

NOTE: The switch function is related to the setting of the rear panel BATT/CHARGE/MAINS switch.

Power ON Position

The instrument will operate from the mains or optional battery supply as selected by the rear panel MAINS or BATT selection. When CHARGE is selected the Power ON position will give full-rate battery charging.

STANDBY Position

(i) With MAINS selected the instrument will be non-operative except for the frequency standard oscillator.

(ii) With BATT selected the battery economy operation will be available.

(iii) If CHARGE is selected the instrument will not charge the batteries.

Power OFF

In the OFF position the charging and operating facilities are switched off, irrespective of the type of power supply.

RESOLUTION Switch

This four position switch selects the appropriate gate time from the time base to give the required resolution. Generally, the switch will be set so that the measurement just fills the display. The display units are indicated by the associated LED's (MHz, kHz, Hz).

INPUT A/B/LF Switch

This switch selects the operational input channel and also the optional LF facility.

CHECK/OPERATE/RESET Switch

In the CHECK position, with INPUT 'B' selected, the 1MHz reference signal is fed through the counting and display circuits; with INPUT 'A' selected a segment check on the display LED's is obtained.

CHECK/OPERATE/RESET Switch (Continued)	OPERATE is the signal measurement mode. When the RESET position is selected and released, the instrument will clear down to zero in readiness for a new measurement. The RESET position is also used in the battery economy operation.
NORMAL/BURST Switch	NORMAL provides continuous measurement with updated display. BURST provides a single shot reading from either an intermittent or a continuous signal.
BATTERY/CHARGE/MAINS	This switch selects the operational power source (battery or a.c. mains). The CHARGE position provides full-rate battery charging when the a.c. supply is connected and the front panel power switch is ON.

INDICATORS

OVERFLOW/STANDBY	The OVERFLOW indicator will illuminate when the count exceeds the capacity of the eight digit display, or when switched to STANDBY.
EXTERNAL STANDARD	Illumination indicates that the instrument is operating from an external frequency standard.
BATTERY LOW	Illumination indicates that the batteries will be exhausted within a few minutes.
GATE/CHARGING	A steady illumination during measurement operation indicates that the counter gating is functioning. The indicator also illuminates while the batteries are charging at the full rate. (The display is off while charging).
MHz; kHz; Hz	Illumination indicates the units of the display.
OVERLOAD	Illumination warns that the input signal on the 'A' channel has exceeded the specified input level (approximately 7V r.m.s.) and that the input is approaching the damage overload level.

REAR PANEL ITEMS

BATTERY/CHARGE/MAINS Switch	See page 1-4.
EXT STD I/P Socket	The input BNC socket for the external frequency standard.
1MHz O/P Socket	A 1MHz reference signal derived from the frequency standard in use is available at this BNC socket.
AGC O/P (Two pin outlet)	Provides indication of Input 'A' signal amplitude. Useful in transmitter tuning.
Data Output/Remote Input Connector	The facilities provided by the 28-way edge connector are listed in Table 1 on page Tech. Spec. (8).
Power Plug/Filter	Contains a mains r.f. filter. A three-core power lead is supplied with the instrument.
Power Fuse	Fuse ratings are marked on the rear panel.
Osc. Adjust	This aperture provides access to the frequency standard calibration adjustment.

CHAPTER 2

OPERATING INSTRUCTIONS

POWER SUPPLY

2.1 AC Supply: Before operating a new instrument, or at a new location, check that the mains voltage selection is correct (see rear panel label). Set the rear rear panel switch to MAINS. When batteries are fitted, trickle charging will occur when the POWER switch is ON.

Battery Supply: Set the rear panel switch to BATTERY. Set the POWER switch to ON and verify that the BATTERY LOW indicator is not illuminated.

FREQUENCY MEASUREMENT (NORMAL)

2.2 (1) Set the controls as follows:-

(a) CHECK/OPERATE/RESET switch to OPERATE.

(b) NORMAL/BURST switch to NORMAL.

(c) INPUT switch to channel 'A' or 'B' or 'LF' as required.

(2) Connect the external signal to the appropriate input socket 'A' or 'B'. The symbol ⚠ advises the user to consult the handbook for further details.

Damage Overload Input Levels

Input 'A'	Input 'B'
10V r.m.s. (overload indication above 7V r.m.s. approximately)	250V r.m.s. up to 10kHz 50V r.m.s. up to 100kHz 10V r.m.s. above 100kHz

(3) Check that the GATE lamp is illuminated.

(4) When using Channel 'A' observe the OVERLOAD indicator. Illumination indicates that the input signal has exceeded 7V r.m.s., and is approaching the damage overload level.

(5) Set the RESOLUTION switch to fill the display, or as required. Read the display in the units indicated by the associated LED's. If required, use the overflow procedure (see next paragraph).

Overflow Procedure

2.3 Enhanced resolution at higher frequencies can be obtained by 'overspilling' one or more of the left-hand digits. First, select a low resolution and record the most significant digits displayed. Then select a high resolution to display the less significant digits to the required resolution. The OVERFLOW indicator will illuminate to show that one or more digits are being overspilled at the longer gate time.

FREQUENCY MEASUREMENT (BURST)

2.4 NOTE 1: The minimum burst duration is 40 ms plus gate time.

2: The user may, if desired, use the BURST mode to obtain a single shot reading from a normal continuous input signal.

(1) Set the NORMAL/BURST switch to BURST. Select the required input channel.

(2) Briefly press the CHECK/OPERATE/RESET switch to RESET. The display will go blank, except the decimal point. When a signal burst is received the display will indicate all zeros, the measurement being displayed at the end of the gate time. The display is then held until the RESET switch is operated again.

BATTERY ECONOMY OPERATION

2.5 (1) Prepare the instrument for battery power supply (para. 2.1) and normal measurement (para.2.2).

(2) Set the POWER switch to STANDBY and briefly press the CHECK/OPERATE/RESET to RESET. The instrument will operate for approximately one and a half minutes and then revert to standby. To repeat the operation press RESET when required.

STANDBY OPERATION

2.6 The operation described in sub-section 2.5(2) can be used with mains powered instruments. It may be noted that when switching from POWER ON to STANDBY the display generally remains on for about a minute before settling into the 'display off' standby condition.

FREQUENCY MEASUREMENT (LF OPTION)

2.7 (1) Set the INPUT switch to the 'LF' position and the other switches as for normal operation.

(2) Connect the external signal to the 'B' input socket (high impedance). The facility is suitable for signal frequencies up to 5kHz, but not with BURST mode.

NOTES: 1. In LF mode a fixed two second gate time is automatically selected and a 100 times improvement in the measurement resolution is obtained.

2. When no input signal is applied it is normal for the instrument to show a few counts.

REMOTE CONTROL OPERATION

2.8 (1) Check that the remote control panel is connected to the 28-way rear panel connector.

(2) Verify that the 9919 A/B/LF switch is not set to LF.

(3) Switch the 9919 POWER switch to ON.

(4) For details of the data on remote control refer to pages Tech.Spec.(8) and (9).

(5) Operate the remote controls as required. If satisfactory gate time and channel selection is not obtained, verify that the Remote Select line (pin R) is at logic '0'.

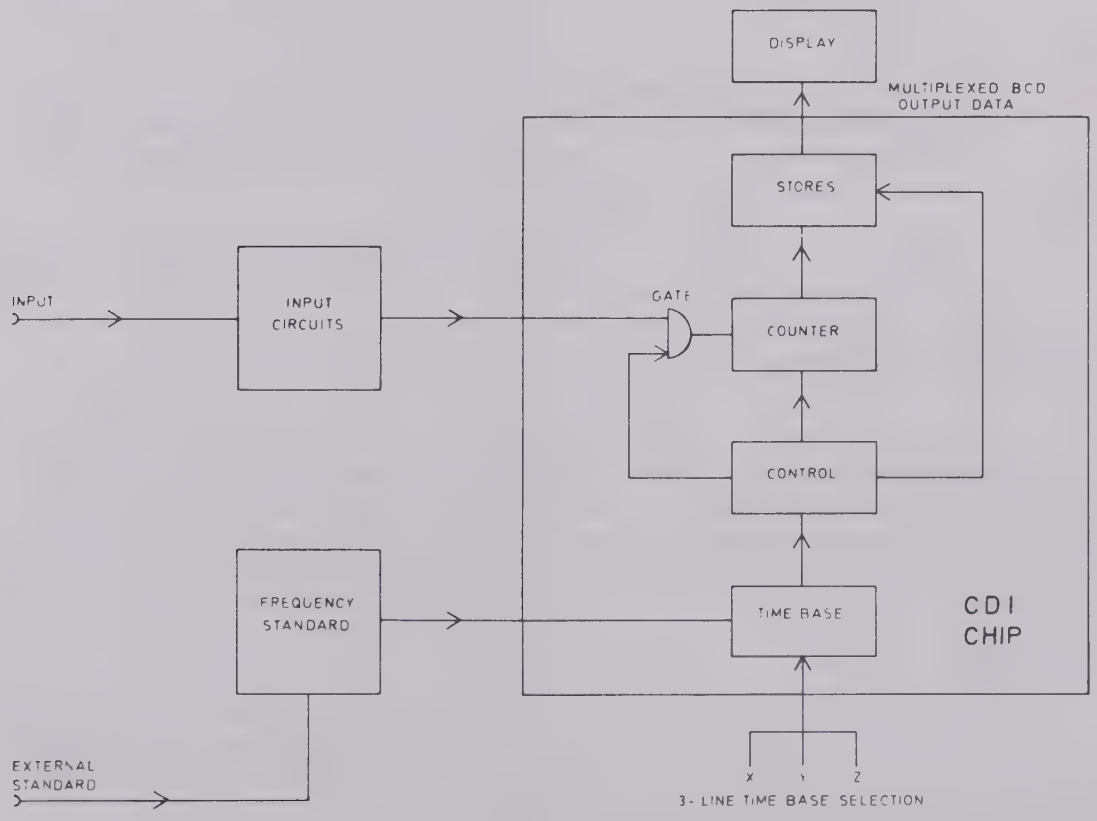
(6) When changing input channel selection, allow a brief amplifier settling time before taking a new reading.

CHAPTER 3

PRINCIPLES OF OPERATION

THE CDI CHIP

3.1 A basic digital frequency meter comprises a chain of decade counters feeding b.c.d. data into latched stores. Counting is controlled via a main gate which is opened for a period determined by the time base. Provision is made for resetting the counter and releasing the data for display. In the 9919, these functions are carried out in the integrated circuit IC4, which achieves large scale integration, using the collector-diffusion-isolation principle. For convenience, IC4 will often be referred to in the handbook as the 'CDI Chip'. Fig. 3.1 is a simplified diagram of the frequency measurement mode, showing the principal functions performed by the CDI Chip.



Basic Frequency Meter Fig. 3.1

GENERAL CIRCUIT FUNCTIONS

3.2 Outside the CDI Chip, other circuit functions are carried out, as follows:-

(a) Input amplification and signal shaping. Overload indication. Input (channel) selection.

(b) An eight-digit display system in bit-parallel byte serial (multiplex) form, with data readout available for external use.

(c) Clock (reference) frequency generation using an unovened 5MHz oscillator circuit, or high-stability temperature controlled oscillator, according to option.

(d) The power supply system operates from either a.c. mains or optional battery pack using re-chargeable nickel-cadmium cells. Trickle charge and full charge facilities are included. 'Charge' and 'Battery Low' indicators are provided. Supplementary power supply circuits provide +24V for the 'A' amplifier and +2V for the CDI Chip. A 'battery economy' facility is provided.

(e) The BURST facility employs circuits which put the counter into the Hold condition with blanked out display. The incoming signal then automatically resets the counter and allows a single measurement to be made, held and displayed.

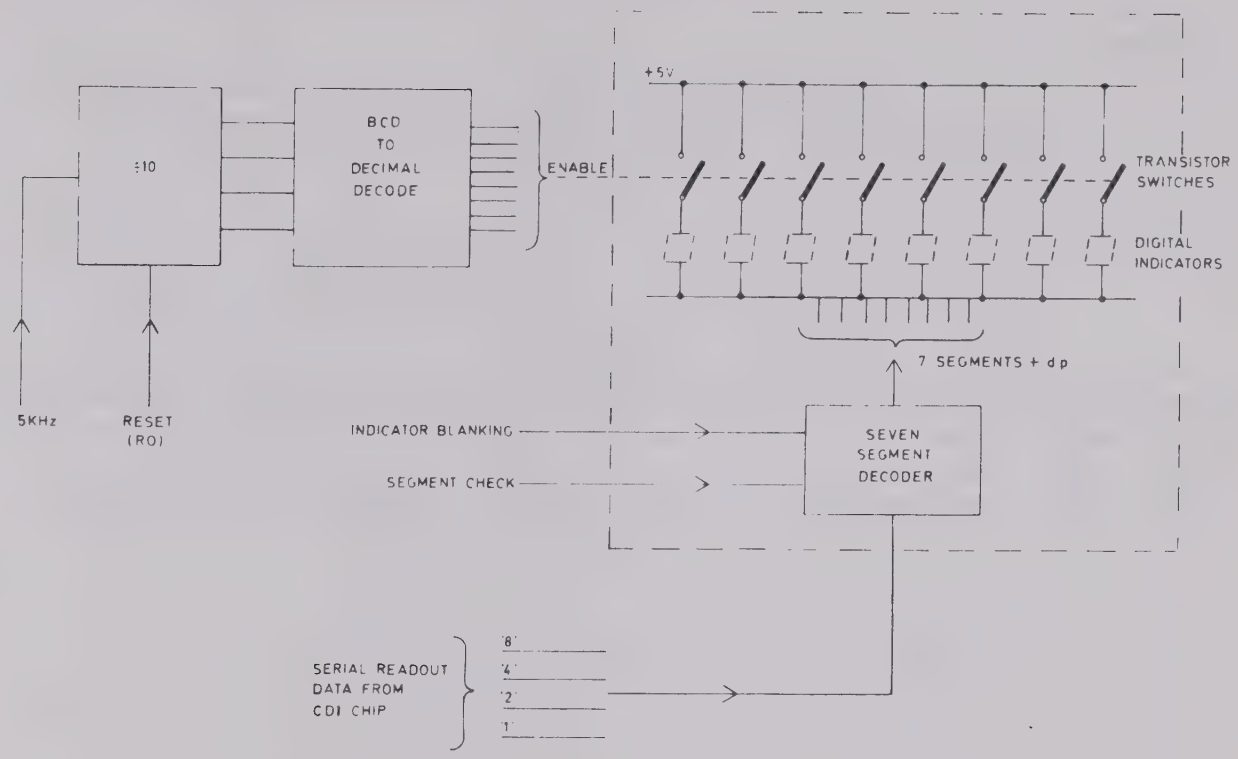
(f) Eight l.e.d. indicators are provided to assist efficient operation. These are described in paras 4.54 to 4.61.

DYNAMIC DISPLAY SYSTEM

3.3 The Display Assembly contains an eight-digit display using light-emitting diodes as numerical indicators. These indicators are driven by b.c.d. data from the CDI Chip, via a seven-segment decoder. Each displayed numeral is formed by illuminating an appropriate number of short straight segments. The numeral '8', for example, for formed from 7 segments, whereas the numberal '3' will require only 5 segments.

Multiplex Readout

3.4 The readout data is fed from the CDI Chip to the Display Assembly via a single four-wire b.c.d. connection. To permit this simple interconnection a parallel-to-serial (multiplex) system is used. The principles are shown in Figure 3.2, although it should be noted part of the system is in the CDI Chip.



Multiplex Display System Fig. 3.2

3.5 In the CDI Chip the data stores feed in parallel into a common b.c.d. four-line output. The store outputs are enabled in turn for approximately 200 microseconds by a 5kHz reference signal, derived from the frequency standard.

3.6 The b.c.d. data is fed to a 7-segment decoder (IC1) in the Display Assembly, which offers the decoded data to the bank of LED digital indicators. The 5kHz reference signal is fed to a BCD/Decimal decoder which 'enables' each display LED in turn for 200 microseconds. A reset pulse (Ro) which is generated in the 10^{6} state of the counter, ensures that the display enable is synchronised with the data store readout. Provision is made via IC1 for a segment check and also for briefly blanking out the display when the system is re-synchronising before commencing a new count.

Decimal Point

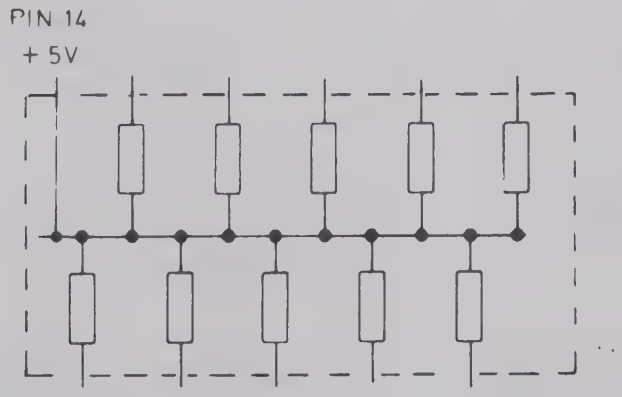
3.7 Decimal point (d.p.) illumination is obtained by encoding the time base control (RESOLUTION) switch logic with the digital indicator 'enable' signals. When operating with the 'A' Input, the decimal point is shifted by one position to compensate for the division-by-ten in the 'A' channel input. A fixed decimal point position is introduced when the optional LF Mode is in use.

Control Information

3.8 A 3-line system is used for time base (gate time) selection. The lines are identified as x, y and z, and the logic coding as it appears at the rear data connector is in Table 2 in the Technical Specification.

Resistor Arrays

3.9 Many of the integrated circuits are 'open collector' types. For these IC's discrete 'pull-up' resistors are provided in the circuit. These resistors may be mounted in a sealed dual-in-line (d.i.l.) package for example R173 (Fig. 5) which has thirteen 10k resistors with a common connection to +5V. Such arrays cannot be serviced and must be changed in the event of a faulty resistor. Fig. 3.3 shows such an array schematically. Another type of resistor array comprises a d.i.l. package containing separate resistors of identical values, for example R2 in the display circuit which contains eight 47Ω resistors.



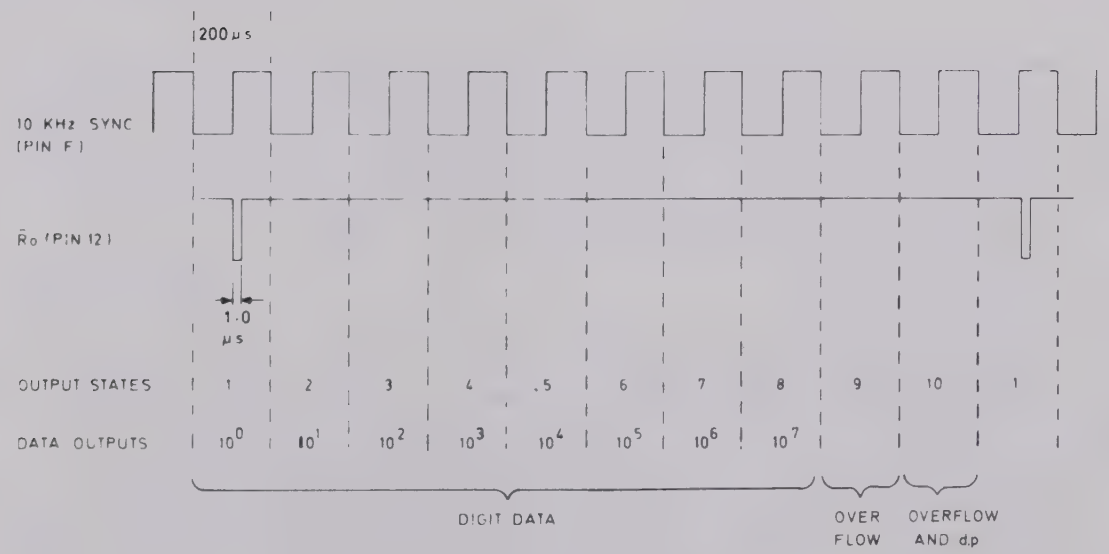
D.I.L. Resistor Array Fig. 3.3

DATA OUTPUT FORMAT

3.10 The b.c.d. output data is available at the 28-way edge connector in a bit parallel byte serial form. The data is sequenced by a 5kHz synchronising signal. The data presentation is delayed 1.0μs from the negative edge of the synchronising signal. An additional synchronising pulse (Ro) determines the first state (10^0 digit). The data output can be converted to parallel format by means of the Serial-to-Parallel Interface Unit (Option 01).

3.11 Fig. 3.4 (not drawn to scale) shows the timing sequence for the ten states. The data on each state is as follows:-

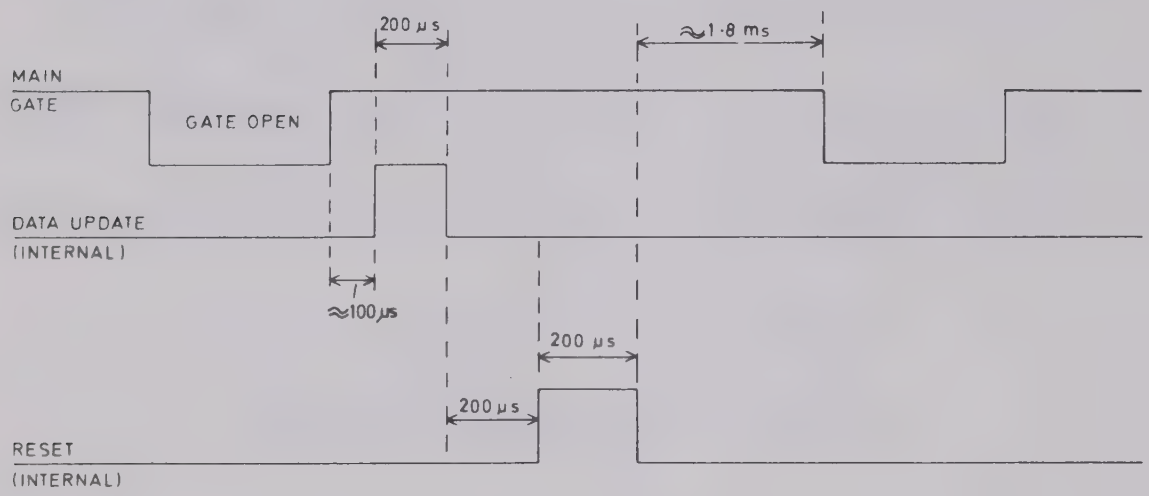
Stages	Facility
1 to 8	Digit (display) information.
9	Overflow for 10^3, 10^4, 10^6 and 10^7 digits on pins D, E, 4 and 5 respectively.
10	Decimal point position in kHz units (relative to directly gated input) plus overflow information for 10^5 digit, via pin 5.



Data Sequence Diagram Fig 3.4

INTERNAL CONTROL SEQUENCE

3.12 Fig. 3.5 shows the control sequence diagrammatically (not to scale).



Control Sequence Diagram Fig.3·5

Control and Information Data

3.13 Data on the correct application of external hold, reset and control signals is given on page Tech. Spec. (9).

CHAPTER 4

TECHNICAL DESCRIPTION

INTRODUCTION

4.1 Apart from some switches and certain items of the power supply, the circuit for the instrument is mounted on one main p.c.b. assembly, with smaller assemblies for the display, reference oscillator and LF Multiplier Option. The part numbers and circuit diagrams are as follows:-

Title	Assembly Ref.	Circuit Figure No.
Overall Circuit and Main (Motherboard) PCB	19-0852	(Fig. 4 (Fig. 5
Display Assembly	19-0853	Fig. 5
LF Multiplier Assembly (Option 09)	19-0797	Fig. 6
5MHz Discrete Oscillator Assembly (Option 04C)	19-0834	Fig. 2

LOGIC CIRCUIT SYMBOLS

4.2 Extensive use is made of integrated circuits (IC's) and these are identified by a number and suffix letter. In the circuit description a particular IC pin will be identified by a reference such as 'IC10a/3', which indicates pin 3 on that particular gate. The logic symbols used in the circuits are those found in most manufacturers IC data sheets to which reference should be made if detailed information is required. The CDI Chip IC4 is, however, obtainable only through the Service Department of Racal Instruments Ltd.

'A' CHANNEL INPUT

Introduction

4.3 The circuit is Fig. 4 at the back of the book. The channel 'A' amplifier operates over the range 80 to 1100MHz with 10mV sensitivity and automatic gain control (a.g.c.). Overload is indicated by an LED and the signal frequency is divided (prescaled) by twenty, then fed to the frequency input of the CDI Chip (IC4/22). Power supplies of +5V, -5V and +24V are used in the 'A' amplifier circuit

Signal Path

4.4 The signal path will be described briefly, with more detailed descriptions commencing at para.4.7. Referring to the circuit in Fig.4 the signal is fed into the main p.c.b. at pin 24/25 thence via C34 to a p.i.n. diode attenuator (para.4.9) and the

input of the thick film amplifiers IC28 and IC21. Note that these amplifiers have a +24V supply.

4.5 From IC21 the signal is fed into parallel paths at C43 and R62. The signal via C43 feeds the a.g.c. detector D17 and D18, and is also used for setting the threshold at which the instrument commences to count (see para. 4.11).

4.6 The signal at R62 is fed to a u.h.f. divide by ten stage IC22. From IC22 the signal is directed via the channel selection logic gates IC13d/IC13a. From IC13a the 'A' and 'B' signals have the same routeing, via the divide by two stage IC9 and amplifiers Q6 and Q7 to the differentiating circuit C24/R43/Q8, which converts the output waveform to narrow positive going pulses. These are gated via IC6a, which is disabled on CHECK and LF, to the Burst Input line, and via IC6c and the level setting resistor R50 to the counter input of the CDI Chip (Fig.5).

'A' Channel Overload Indication

4.7 Although the fast acting a.g.c. system can cope with short term overloads. The input circuit is not intended to withstand prolonged overload conditions, therefore an overload warning indication is provided by the following components:-

(1) The detectors D15 and D16 with capacitor C38.

(2) The operational amplifier IC35b.

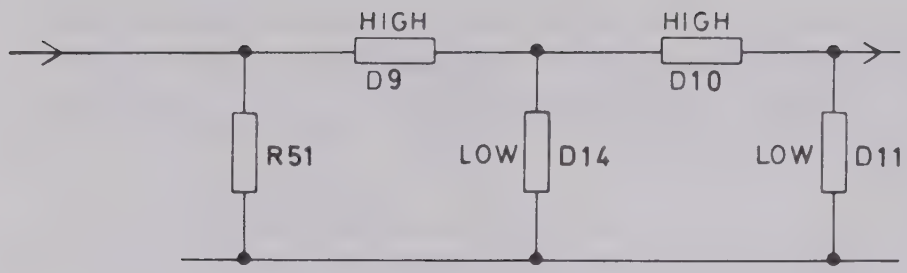
(3) Transistor Q10 which drives the front panel OVERLOAD indicator.

4.8 The 'A' input signal at pin 24 is fed via C36 to the detector D15/D16 and the rectified signal is applied to IC35b/7. If the input signal level rises above approximately 7V r.m.s. the output at IC35b/10 will go high enough to turn on Q10, causing the overload l.e.d. to illuminate.

PIN Diode Attenuator

4.9 The attenuator operates on the principle that the impedance of a diode varies according to the applied bias current. The series elements in the attenuator are diodes D9 and D10, and the shunt elements D14 and D11. Fig. 4.1 below shows the network theoretically, with the diodes represented by resistors. The impedance states refer to a condition of high attenuation.

4.10 If the a.g.c. voltage drives the anode of D14 positive, then current will flow in R52 and the cathodes of D9 and D10 will be reverse biased, causing a high series impedance. The current in R53 will flow through D11, causing a low shunt impedance. A low level of a.g.c. voltage will produce the opposite conditions, and there will be variable attenuation over the rest of the a.g.c. range.



Theoretical P.I.N. Diode Attenuator Fig. 4.1

Counter Enable Circuit

4.11 The counter in the CDI Chip IC4 (Fig.5) is inhibited if the 'A' input signal is too low for reliable counting. This is determined in IC20a and the threshold is preset by potentiometer R71. The signal from IC21 is fed via detectors D17/D18 to IC20a/1. The reference voltage at IC20a/2 is preset by R71. If the input signal level is satisfactory, the output at IC20a/12 will be a '1' which will enable the counter in IC4. Instructions for setting-up R71 are given in Chapter 5.

Automatic Gain Control

4.12 At low signal levels the cathodes of D17 and D18 will be at approximately 0V. As the signal amplitude increases, the voltage at the cathode of D18 (and also at IC20b/7) will become increasingly negative. When the voltage at IC20b/7 is equal to or more negative than IC20b/6, an output will be applied from IC20b/10 to Q12, which feeds current into the p.i.n. attenuator at D14. The a.g.c. voltage across R75, is accessible at the two-pin outlet on the rear panel, providing a useful indication for purposes such as transmitter tuning.

'B' CHANNEL INPUT

Signal Input

4.13 Reference should be made to the circuit diagram Fig.4. Signals in the range 20Hz to 100MHz are applied to the front panel 'B' input socket and fed to the 'B' amplifier via pins 27/26 on the Main PCB.

'B' Channel Amplifier

4.14 Referring to Fig.4, the 'B' amplifier has a high impedance FET input (Q1) with overload protection by the clipping resistor R3, together with the gate-drain junction and diode D1. The output from Q1 source drives a wideband amplifier IC33 via emitter follower Q2.

4.15 From IC33 the signal is fed via Q3 and emitter follower Q26 to the Schmitt Trigger shaper IC17C, and also, via C13, to an a.g.c. circuit formed by D4/D5/IC35a/D2 and associated components. The level at IC35a/12 is monitored in the 'B' channel performance check (Chapter 5). The signal at Q26 emitter is also fed, via R21, to the LF Multiplier p.c.b., when fitted.

4.16 The signal from IC17b/3 is fed via the input channel selection gate IC13c to gate IC13a, at which point the 'A' and 'B' signals follow a common path. The signal now passes via IC9 and Q6/Q7/Q8 as described in para 4.6.

INPUT SELECTION

Channel Switching

4.17 The required A or B input channel is selected by the front panel INPUT switch (Fig.5) which is part of the Display Assembly. Referring to Fig.4, the INPUT switch line selects the required amplifier by controlling the +5V supply via Q4 ('B' amplifier) or Q15 and Q13 (for the 'A' amplifier). The input selection also controls a 24V generator for the 'A' amplifier as described in the next paragraph.

24V Generator

4.18 The +24V for IC28 and IC21 is generated in the circuit Q9/T1, rectified by D6/D7 and smoothed by C26/C84/L5/C42. The generator drive to Q9 is the 500kHz standard signal, supplied via IC7d. The generator develops a rectified +19V which is combined with the +5V rail to provide +24V to IC21 and IC28.

4.19 The 24V generator is controlled by the INPUT switch S2 (Fig.5) which inhibits IC7d when channel 'B' or LF mode is selected, thus cutting off the drive to Q9. The inhibit is removed when 'A' channel is selected.

CHECK/OPERATE/RESET SWITCH S50 (Fig.4)

4.20 This switch applies a '0' to the CHECK or RESET line, except when the Remote Select line is at '0', in which case IC34a/2 goes to '1' and inhibits the switch selection.

OPERATE Mode

4.21 There is no earth connection and the line joining R83 to gates IC5a, IC25d, IC5d, IC6b and IC6a is at '1' state.

CHECK Mode

4.22 With S50 set to CHECK a 0V connection is made by the switch and the following actions can occur:-

(1) Lamp Test

A '0' state on IC5a applies a '1' to IC5b (Fig.5). Provided the INPUT switch is at '1', IC5b/6 and hence IC1/3 will go to '0', causing the segment decoder to illuminate all segments in the display l.e.d's.

(2) Self Check Signal

A '0' is applied to IC6b/3 and IC6a/1 which inhibits the LF, 'A' and 'B' signal gates. At the same time the '1' at IC5a/3 enables IC5c, thus feeding the 500kHz standard signal via IC6c to the CDI counting circuits.

RESET (Manual)

4.23 When the spring-biased switch S50 (Fig.4) is pressed to the RESET position the counter will go to the Hold condition for the Time that the switch is held down. Reset occurs at the moment of release. The various logic conditions produced at the CDI Chip IC4 (Fig.5) are as follows:-

Counter Mode	IC4 Pin 13
Hold	'1' state
Free-running	'0' state
Reset	Occurs on the transition from '1' to '0'.
	IC4 Pin 4
Latch	'1' state
Unlatch	'0' state

The counter normally operates in the latched mode, but is unlatched during the reset transition. The circuit action is as follows.

Manual Reset Action

4.24 When switch S50 (Fig.4) is held in the RESET position, a '0' is applied to the monostable IC32a/5. This produces a '1' at IC32a/7 and, via IC31a and IC16a, a '1' at IC4/13, thus putting the counter into the Hold condition. When switch S50 is released from the RESET position the transition from '1' to '0' at IC4/13 causes the counter in the CDI Chip to reset. At the same time this transition is inverted in IC7a and clocks the monostable IC32b, which via IC16b produces a '0' at IC4/4 for the period of the monostable pulse, thus briefly unlatching the data stores in the CDI Chip to allow the display to be reset to all zeros at the start of the new count.

4.25 The Hold/Reset levels at IC4/13 are fed out via IC11c to give the inverted levels at Pin 13 of the rear data output connector.

EXTERNAL HOLD

4.26 IC4/13 requires a '1' level to put the counter to Hold mode, therefore an external '0' must be applied to pin 6 of the rear data connector. This is inverted in IC31c. Reset will occur when the external level changes from '0' to '1'.

TIME BASE (RESOLUTION) SELECTION

4.27 The time base divider chain in the CDI Chip is programmed by logic signals applied to the x-y-z inputs of the chip (Fig.5). The time base control code at pins 8,9 and 10 of the CDI Chip is as follows:-

Gate Time (seconds)	Resolution		Control Code *		
	'A'	'B'	X	Y	Z
.02	1kHz	100Hz	1	0	0
0.2	100Hz	10Hz	0	1	0
2	10Hz	1Hz	1	1	0
20	1Hz	0.1Hz	0	0	1

* NOTE: The logic levels at the rear data connector and at switch S, are the reverse of those at pins 8, 9 and 10 of the CDI Chip.

4.28 The x-y-z code is also used in determining the decimal point position as described in para.4.46. For this purpose only one line must be at logic '1' and this is ensured by suitable encoding in the gate and inverter network IC14d, IC15d, IC25c and IC14c.

RESOLUTION SWITCH S1

4.29 For local operation the switch has a 0V connection on the wiper, tag 6, via the inverter IC34e. The logic levels produced by operation of the switch are inverted by IC25a, IC25b and IC15c and applied to pins 8, 9 and 10 of the CDI Chip in accordance with the code in Table 2 (Page Tech.Spec(9). Transistor Q21 is conducting so long as the Remote Select line is not at '0' state.

4.30 For remote control, pin R of the rear data connector must be held at logic '0'. This turns off Q21 and disables switch S2 by putting a '1' on IC34e/10. The reason for turning off Q21 when on remote is to prevent the linking of the 'y' and 'z' lines which occurs at the switch wafer on certain positions

MAIN GATE

4.31 Counting is controlled by the main gate within the CDI Chip (see page 3-5). The gate waveform, which goes negative when the gate opens, is fed out on IC4/19, inverted in IC7c and then applied as follows:-

(1) To pin H on the rear data connector for use as an external indicator.

(2) To Q37 to illuminate the GATE/STANDBY l.e.d. indicator.

(3) At the end of each main gate period the negative edge is passed via R129/C70 to transistor (j) in IC30, which then produces a pulse fed via IC19d and pin 11 of the display board connector to blank the display for approximately 1ms whilst the multiplexed display is re-synchronising with the circuit in the CDI Chip.

BURST MODE

Summary

4.32 When the MODE switch is set to BURST the counter in the CDI Chip is automatically set to Hold and the display is blanked out (except the decimal point). When a signal is received it triggers a circuit which causes the counter to reset and commence a single shot measurement; at the same time the data stores are briefly unlatched, allowing an 'all zeros' display to appear while the measurement is in progress. The updated display then appears at the end of the gate time. To prepare for a new measurement the RESET switch is pressed and released; this blanks out the display and clears the counter for the next burst input.

Burst Circuit Description

4.33 The logic requirements at Pins 13 and 4 of the CDI Chip as given in para.4.23 are relevant to this description.

4.34 When the MODE switch 1S1 (Fig.4) is set to BURST (provided LF is not selected) a '1' is applied to IC31b/3 (Fig.5) which enables the gate and, via IC31c puts a '1' on IC4/13, thus putting the counter into the Hold condition. The Burst Select logic also puts a '1' on IC19a/2 which applies a '0' to the blanking input (pin 4) of the 7-segment decoder IC1 on the Display p.c.b. when the manual reset is pressed.

NOTE: If LF operation is selected Q16 (Fig.4) will be turned on, thus grounding the Burst Select line and preventing Burst operation.

4.35 The other inputs to IC31b are already at '1' because IC31/5 is connected to the junction of R103/R108 (about +2.5V) and IC31b/4 receives a '1' from Q23 collector (see para.4.39) via inverter IC27b.

4.36 After selecting BURST mode, the operator selects manual reset, this presets the Dual-D bistable IC12b, but does not disturb the Hold condition of the counter. The manual reset produces a '1' at IC12b/9 which is applied to IC19a/1. As IC19/2 already is at '1' on the Burst Select line, the resultant '0' from IC19a/3 blanks the display digits via the 7-segment decoder IC1. The system is now ready to receive the burst signal input.

4.37 Burst Signal Action When a signal is received on the Burst Input line (Fig.5) it clocks the bistable IC12b, which changes state. The 'Q' output goes to '0', but due to capacitor C62 this pulls the 'D' input of IC26a down to '0' for only a short period. When C62 is charged the next clock (5kHz) signal at IC26a/3 clocks the $\overline{Q}$ output of IC26a/6 back to '0', which via IC31b/5 and IC31c pulls IC4/13 down to '0' giving the reset transition which starts a new measurement.

4.38 The '0' at IC4/13 is also applied via inverter IC7a to trigger the monostable IC32b which, for the duration of the monostable period, pulls IC4/4 down to '0', thus briefly unlatching the display to allow the 'all zero' reset display to appear while the count is in progress.

Function of Q23

4.39 Transistor Q23 and associated diode D23 provide an interlock facility which ensures that the counter and multiplex system is correctly set for 'burst' reception. Q23 monitors the output of IC24 via Q22 and the detected signal via the gating path IC27 IC31b and IC31c holds the counter in a free-running condition until IC24 is operating in the correct sequence.

4.40 A secondary function of Q23 is to blank out the display if the 5kHz multiplex reference signal fails. Such failure would cause a display l.e.d. to be continuously illuminated. Any loss of drive from IC24 to Q23 will apply a '0' to the 7-segment decoder IC1, thus blanking the display.

DATA OUTPUT AND DISPLAY SYSTEM

Data Output Format

4.41 Refer to the Supplementary Data in the Technical Specification at the front of the book for a summary and diagram of the data output format.

Multiplex Readout and Display

4.42 The Display Assembly contains an 8-digit readout system using light-emitting diode (l.e.d.) numerical indicators. The display data is fed from IC4 on pins 15 to 18, this 4-way output being fed from a parallel-to-serial (multiplex) system within the CDI Chip, to the 7-segment decoder IC1 on the Display Assembly.

4.43 In the multiplex system the b.c.d. outputs from the data stores are fed in sequence on to the 4-way output. This is determined by a 5kHz synchronising signal (derived from the frequency standard) which interrogates each decade store in turn for a period of 200μs. The same 5kHz signal is used (via IC24) to 'enable' the appropriate l.e.d. in the display.

4.44 The system is set by a (Ro) signal which occurs in the '0' (10^{o}) state of the data output at IC4/14. This sets IC24 to the 10^{o} state, and, via transistor IC29a, turns on Q28. This enables the 10^{o} digital indicator DI1 which displays the digit determined by the 7-segment decoder IC1. The other display l.e.d's Q29 to Q35 are then enabled in sequence for a period of 200μs each, via transistors IC29(b) to (e) and IC30(f) to (h).

Decimal Point Selection

4.45 The decimal point (d.p) in the required display l.e.d. is illuminated by turning on the common d.p. cathode driver transistor Q25 and IC30k at the same time as the anode of the required digit is enabled. The links LK1 and LK2 in the collector circuit of IC30k are to permit the use of different types of l.e.d. indicator. See Parts List 1 for details.

4.46 The decimal point position is determined by two factors: (a) the Input channel selection, which takes account of input prescaling, and (b) the setting of the RESOLUTION switch. The actual illumination of the decimal point is then determined by the multiplex enable signals on five of the eight lines from IC24.

4.47 Decimal point selection is exercised via the NAND gates IC23a-d and IC19c which control Q25 via the pull-up resistor R128. Except when a decimal point is required, Q25 will be turned off because one of these gates will have an output at '0', thus holding down the base of Q25.

4.48 When Input 'B' is selected at switch S2, a '0' will be applied via inverter IC27c to pin 1 of the quad 2-to-1 line multiplexer IC18. This allows the data on pins 2,5,14 and 11 of IC18 to be transferred to pins 4,7,12 and 9 respectively. When Input 'A' is selected IC18/1 goes to '1' and the data transfer is from pins 3, 6, 13 and 10. This has the effect of shifting the decimal point by one position to allow for the ÷10 prescaling of the input signal on Input 'A'.

4.49 For example, assume that with Input 'A' selected the RESOLUTION switch setting requires the 10^{3} decimal point to be displayed. The INPUT switch S2 applies a '1' to IC18/1 and the RESOLUTION switch together with the encoding network IC14d/IC15d/IC25c/IC14e puts a '0' on IC18/3, which transfers a '1' to IC23c/10. The lines from pins 7, 12 and 9 of IC18 will all be at '0'. Pin 15 of IC18 is held at '0' which disables IC19c. (see para.4.52 strobe). Thus, in this example, only IC23c is holding the base of Q25 low.

4.50 The IC23 gates are also controlled by the multiplex reference 'digit select' signals from IC24. These lines are at '1' except when they are receiving the 5kHz digit select. If, for example, the 10^3 digit line is enabled (IC24/7), a '0' is enabled (IC24/7), a '0' is applied to IC23c/9 thus allowing the common output from IC23 rise to '1', which turns on Q25 during the 10^3 enable period, thus turning on the 10^3 digit decimal point.

Strobe (LF) Time Base and DP

4.51 The 'strobe' line is relevant to the LF Multiplier option only. When either local or remote LF mode is in use, a '0' is applied to inverter IC27a/1 (Fig.4) which puts a '1' on IC25d/13. Since IC25d/12 is at '1' (switch S50 at OPERATE) a '0' is fed from IC25d/11 to the inputs of the time base encoding gates IC25a and IC25b (Fig.5) and a '1' to IC15c via inverter IC14f. This forces the time base to a two-second gate time, irrespective of the setting of the RESOLUTION switch.

4.52 From IC14f/12 the '1' state strobe signal is fed to IC18/15, thus holding all outputs from the multiplexer at '0', which disables the gates IC23a to d. The '1' state is also applied to IC19c/9 which produces a 1' state output whenever the 5kHz digit select signal from IC24/4 falls to '0', thus turning on Q25 to produce the fixed (LF) decimal point at the appropriate time.

4.53 The '1' state strobe is also applied to the encoding network IC11a, IC14a, IC15b, IC11b and IC15a, in order to change the output b.c.d. data to conform with the x100 frequency multiplication when the LF Multiplier option is in use.

LED INDICATORS

EXTERNAL STANDARD Indicator (LP1)

4.54 This l.e.d. illuminates when an external frequency standard is connected, see para. 4.63.

OVERLOAD Indicator (LP2)

4.55 Refer to para. 4.7.

MHz and kHz (LP3 and LP4)

4.56 Referring to Fig.5, on normal measurement mode (not LF) Q1 is conducting, therefore the illumination of LP3 and LP4 depends on the logic level on the time base selection (Z) line at IC15c/10. Reference to Table 4 in para 4.27 shows that the Z code is '0' except on the 20 second gate time. When IC15c/10 is '0' this is fed through inverters IC27d and IC34d to turn on the MHz l.e.d. When 20 second gate is selected, however, IC34d/8 goes to '1' and IC27d/9 to '0', thus turning off LP3 and turning on LP4.

Hz Indicator (LP5)

4.57 Referring to Fig.5, when either local or remote LF mode is selected, a '0' is applied to the base of Q1 which turns off, thus applying +5V across LP3 which illuminates to indicate that the display is in Hz units.

OVERFLOW/STANDBY Indicator (LP6)

4.58 The b.c.d. data output from the CDI Chip is fed to the display assembly, and also via an encoding network to appear as inverted b.c.d. levels at pins D, E, 4 and 5 of the data output connector. The 8 line of this b.c.d. data is applied to the inputs (IC10c and IC10d) of a set-reset bistable IC10a/IC10b whose output is connected via R172 to the l.e.d. LP6. When the 8th state (10th decade) of the counter overflows, a signal is sent from IC24/9 which triggers IC10a/IC10b and turns on LP6. The STANDBY function is described in para.4.69.

GATE/CHARGE Indicator (LP7)

4.59 The main gate waveform from the CDI Chip, inverted in IC7c, turns on Q37 to illuminate LP7. Although Q37 conducts only when the main gate is open, the 'off' intervals are too brief to be seen and the illumination appears to be continuous.

4.60 When the rear panel switch is set to CHARGE, with mains power switched on, LP7 will be illuminated continuously, Q37 being held on via R140. This indication shows that 5V power is available to the charging circuit.

BATTERY LOW Indicator (LP8)

4.61 Refer to paras 4.83 and 4.84.

FREQUENCY STANDARD SIGNALS

Clock Frequency

4.62 The clock (reference) frequency used in the CDI Chip is 500kHz. This frequency is derived from the following alternative sources:-

(1) The internal 5MHz frequency standard is fed via Q24 (Fig.5) and IC7b to the CDI Chip at IC4/5. This is divided in the Chip, to 500kHz and fed out via IC4/6 for driving the 24V generator (para.4.18) and to provide a self-check signal. The 5MHz is also fed to IC2 (Fig.4) for division by five. This provides the standard output via IC1c and IC1b to the rear panel 1MHz O/P socket SK53.

(2) The 1MHz external standard input is fed via the rear panel socket EXT STD I/P to pins 42/41 (Fig.4), thence to Q18 which feeds the 1MHz signal via gate IC1b to the rear panel 1MHz O/P socket. The output

from Q18 also goes to IC2/14 for division by two, thus providing the 500kHz external standard from IC2/12 to the CDI Chip. The divide by five section of IC2 is inhibited by the feedback via IC1d/IC1a.

External Standard Operation

4.63 The 1MHz external standard signal at Q18 collector (Fig.4) is detected by D21/C53 and the resultant d.c. level inhibits IC1c, thus cutting off the internal 1MHz output, and at the same time turning on Q17, thus illuminating the EXTERNAL STANDARD l.e.d. on the front panel. The divide by five section of IC2 is inhibited by the feedback via IC1a, which is enabled by the rectified signal from D21/C53. The CD1 Chip automatically changes to external standard operation when the 500kHz clock is received at IC4/20 (Fig.5).

FREQUENCY STANDARD OPTIONS

4.64 These are listed in the Technical Specification as 04A, 04B and 04C. The instrument is normally supplied with 04B. The circuit and component layout diagram for Option 04C is Fig.2. No technical information is provided for the ovened oscillators as these should be serviced only by Racal Instruments Ltd, or authorized agents. A frequency calibration procedure is given in Chapter 5.

POWER SUPPLY

Introduction

4.65 The power supply circuit operates from a.c. mains supply, or from optional internal batteries, and provides the following facilities:-

(1) +5V and -5V stabilized supply rails.

(2) Trickle charging and full-rate charging of batteries, if fitted.

(3) Standby indication and indication of low battery voltage.

(4) Battery economy operation.

Elsewhere on the main p.c.b. are two other subsidiary circuits; a +2V stabilizer, Q19/Q20 which supplies the CDI Chip and a 24V generator which is described under Input Selection (para. 4.18).

AC Supply

4.66 Referring to Fig.5 the a.c. supply is fed in via a 3-pin combined plug and r.f. filter on the rear panel, thence via the anti-surge fuse FS50 to the transformer T50. The transformer tappings are arranged to suit the local supply voltage as shown in Fig. 5.1 in Chapter 5. The output at secondary winding 'A' is rectified to +5V nominal by the potted bridge rectifier D50, which is mounted on the rear panel for adequate heat dissipation.

4.67 The -5V supply is provided by the discrete diode bridge D31-D33 with fuse protection on the negative rail at FS1 (this fuse must be a normal quick action type).

+5V Switching

4.68 The +5V supply to the instrument is switched by the POWER switch S61 using the series transistor switch Q50. The base of Q50 is connected via R135 to the POWER switch S51, such that in the ON position of S51 the base is earthed, thus turning on Q50. The removal of the earth in the STANDBY and OFF positions of S51 turns off Q50 and cuts off the +5V supply (except when Battery Economy mode is operative).

Standby Indicator LP6

4.69 The OVERFLOW indicator also serves as a standby indicator. The anode of LP6 is connected to the emitter side of Q50 and thus receives +5V(H) even though the main +5V rail is cut off. The current is LP6 has a path to earth via R3, which illuminates the LED. When full +5V power is restored, however, this path is closed and LP6 is extinguished.

+5V Stabilization

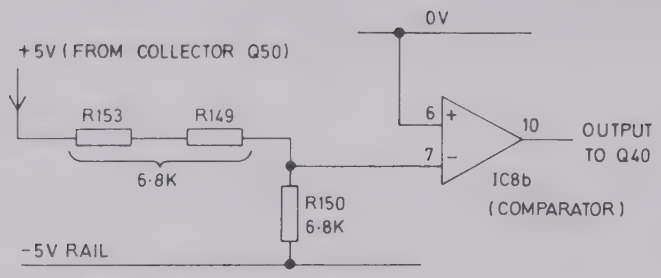
4.70 When POWER is switched to ON the switch contact S51b connects the anode of zener diode D27 to the unsmoothed negative side of rectifier D50. This turns on Q39.

4.71 When Q39 conducts it turns on Q42 which draws current through the reference zener diode D29. The reference voltage is applied to the inverting input of the comparator IC8a/2 and is compared with the voltage from the 0V rail at IC8a/1. Any difference produces an output at IC8a/12 which, via Q38, regulates the current in Q51.

-5V Stablization

4.72 The reference for the -5V rail is derived from the stablized +5V at the collector of Q50, the comparison being made in the comparator IC8b, with regulation by Q52. (See Fig. 4.2).

4.73 Fig. 4.2 below shows the basic connections to the input of comparator IC8b.



-5V Stabilizer Fig.4.2

4.74 Provided the voltage on the -5V rail is equal to that on the +5V rail, IC8b/7 will be at 0V. This is compared with the reference 0V at IC8b/6. Any difference will generate an output voltage at IC8b/10 which will drive Q40 to regulate the current in the series transistor Q52. Transistor Q41 provides overload protection when using the optional battery supply. (See para. 4.82).

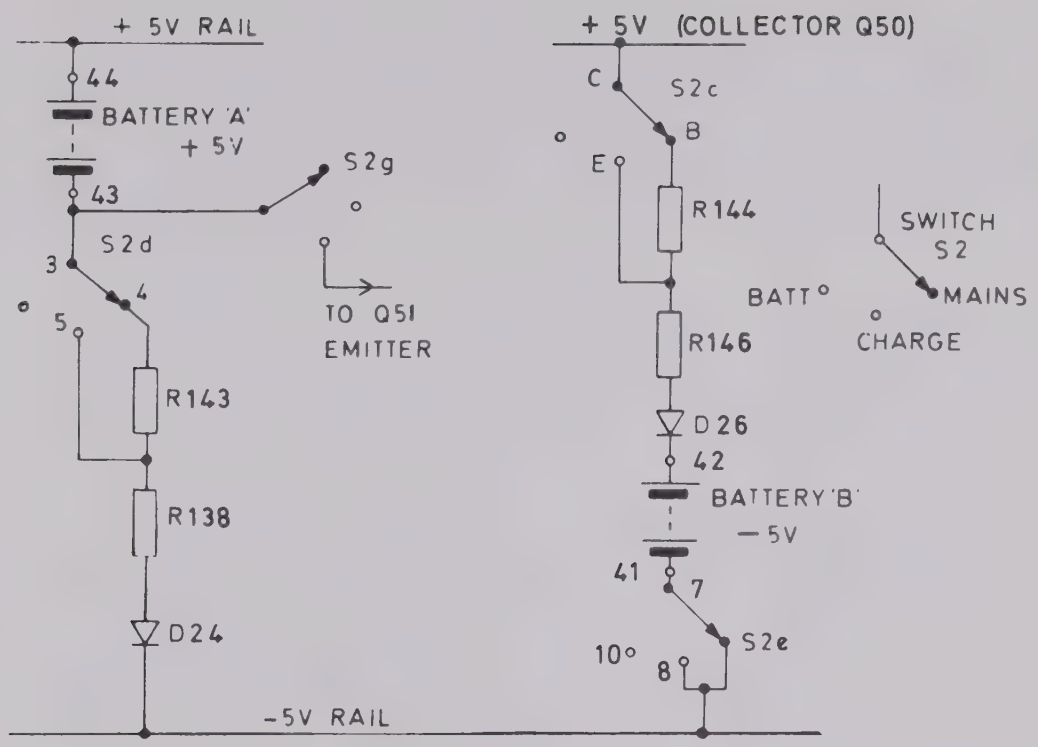
Battery Economy Operation

4.75 When the Power switch is at STANDBY the +5V supply rail is cut off because Q50 is non-conducting. If the CHECK/OPERATE/RESET switch (Fig.4 S50) is depressed an earth is applied via D25 to the junction of R141/C71. This rapidly discharges C71, causing the output of IC3b/10 to change from negative to positive. This turns on Q36 which feeds current into Q50 base, thus turning on the +5V supply to the instrument.

4.76 Q50 will conduct until C71 has re-charged, which takes approximately one and a half minutes. The +5V rail then reverts to the standby condition with Q50 cut off. This arrangement operates with either mains or battery power supply, but its purpose is battery economy.

Battery Charging

4.77 Batteries (if fitted) are trickle charged whenever the instrument is operating from the mains supply. For charging, each battery is connected between the +5V and -5V power rails, as shown in Fig. 4.3. The diodes D24 and D26 prevent discharge of the batteries if the mains supply is disconnected with the instrument switched on.



Battery Charging Circuit Fig. 4.3

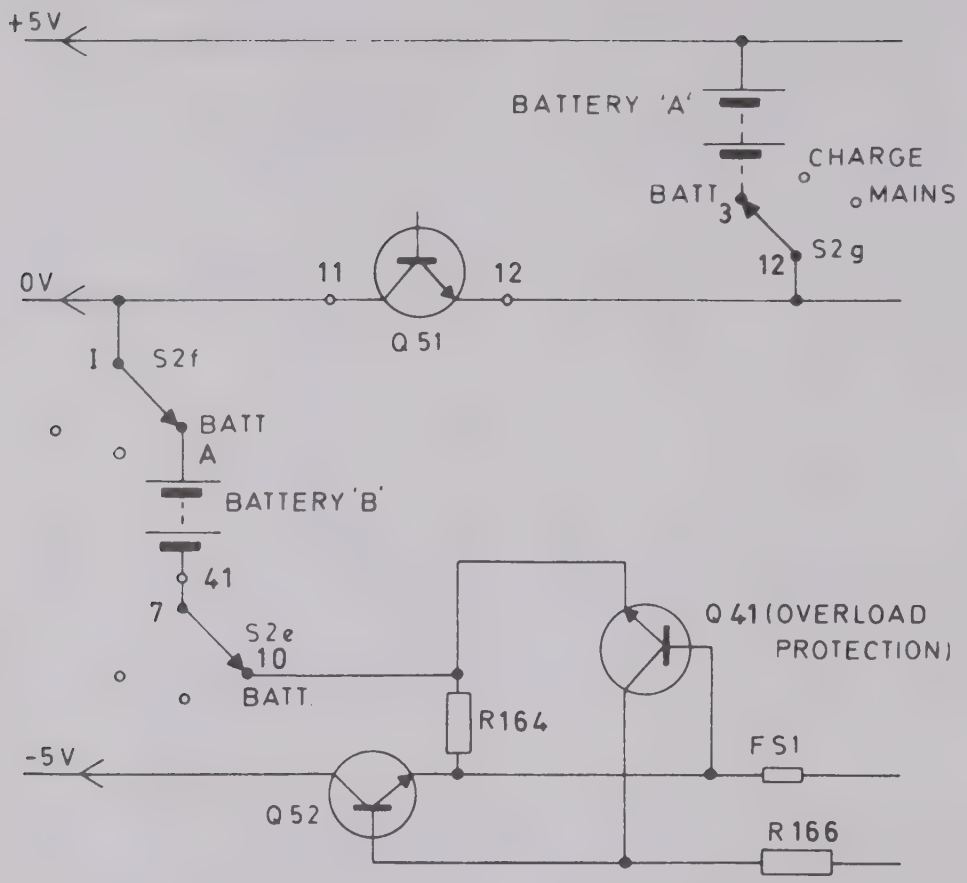
4.78 For full-rate charging the switch bypasses R143 and R144 which increases the current by approximately ten times.

Charge Indicator LP7

4.79 The indicator LP7 illuminates when switch S2 is in the CHARGE position, thus indicating that power is available to the charging circuit. The anode of LP7 is connected to the stablized +5V rail at the collector of Q50. The same +5V supply turns on Q37 which illuminates LP7.

Battery Powered Operation

4.80 When switch S2 is set to the BATTERY position the contacts S2c and S2d disconnect the charging paths. The negative side of battery 'A' is connected via contact S2g to Q51 emitter. (See Fig. 4.4).



Battery Power System Fig. 4.4

4.81 The 0V rail at Q51 collector is connected via contact S2f to the positive side of battery 'B'. The negative side of battery 'B' is connected via the low resistance R164 to Q52 emitter.

4.82 Transistor Q41 provides overload protection to the negative battery. In the event of an overload, Q41 will turn on, thus shunting the base current away from Q52 and shutting off the regulator path.

Battery Low Indicator LP8

4.83 The Battery Low indicator illuminates when the volt drop across the series regulator Q51 falls to less than 0.5V (approximately). The sensing component is IC3a.

4.84 Resistors R165 and R163 are connected from the +5V rail through the POWER switch S51 to the emitter of Q51. The junction of R163/R165 is connected to the inverting input at IC3a/2. The non-inverting input IC3a/1 is connected direct to the collector of Q51. Provided the voltage at Q51 collector is more than about 0.5V positive relative to the emitter there will be no output from IC3a and LP8 will not illuminate. If the lamp comes on it indicates that only a few minutes of battery life are remaining and re-charging is essential.

Over Discharge Protection (D14)

4.85 The Battery Low indicator informs the user that the batteries are in need of re-charging. If this warning is disregarded the instrument will shut itself off after a few minutes to prevent over discharge of the batteries. This is arranged by Q39 and D27.

4.86 R160 and D27 are connected across Battery 'A' (via S51 and S2g). If the voltage falls below about 5V, Q39 will start to turn off which will cause Q42 to turn off. Reference diode D29 will become ineffective, thereby removing the reference voltage. The voltage of the positive rail will fall and the instrument will cease to draw current.

LF MULTIPLIER OPERATION (OPTION)

Signal Path

4.87 The signal for the LF Multiplier is taken from the collector of Q3 in the 'B' amplifier (Fig.4) and processed in the LF Multiplier p.c.b., after which it is fed back to the main p.c.b. at pin 33 and directed through the channel selection gates IC6b and IC6c, where it follows the common input path to the CDI Chip via R50.

LF Mode Gating

4.88 When the INPUT switch (or remote control) is set to 'LF' a '0' is applied to the LF remote line which has the following effect:-

(1) It turns off Q1 (Fig.5) and thus illuminates the 'Hz' indicator l.e.d. LP5.

(2) It applies a '1' via IC5d to the base of Q16, which turns on and grounds the Burst Select line, thus inhibiting Burst operation while on LF.

(3) It disables gate IC6a, thus inhibiting the normal 'B' channel signal from Q8 and also the 'A' channel signal.

(4) It applies a '1' via IC27a, which enables IC6b and releases the LF multiplier signal at IC6b/4. At the same time it produces a '0' at IC25d/11 which is fed via the strobe line to the time base selection circuits (Fig.5) to force the time base into a two second gate time. It also forces the decimal point circuit to give a reading in 'Hz'.

LF Remote Control

4.89 To select LF mode remotely, a '0' state is applied to pin N of the 28-way data output connector. It is important NOT to select LF on the 9919 INPUT switch when remote LF is in use.

LF MULTIPLIER ASSEMBLY 19-0797 (Fig.6)

Principle

4.90 Frequency multiplication is achieved by a voltage controlled oscillator which by means of a link can be set to run at either 50 times or 100 times the input frequency. The divided oscillator frequency is phase-compared with the input frequency to provide fine control of the oscillator frequency.

Circuit Description

4.91 The LF signal is fed from Q3 in the 'B' amplifier (Fig.4) into the LF Multiplier p.c.b.. Referring to Fig.6, the signal is fed via C1 into the Operational Amplifier IC1, which functions as a Schmitt Trigger. With an input of approximately 400mV peak-to-peak applied to IC1 an output of approximately 6V peak-to-peak will be fed into IC2/14.

4.92 IC2 contains a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL). The factors controlling the oscillator frequency are:-

(1) The voltage on pin 9 of IC2.

(2) The resistance between pin 11 and the negative rail.

(3) The capacitance between pins 6 and 7.

(4) The output of the phase comparator at pin 13.

4.93 The oscillator output at IC2/4 is fed via Q3 to a divider chain (IC3 and IC4). The divided signal is fed back via Q2 to pin 3 of IC2, where it is compared in phase with the original signal in pin 14. This phase comparison voltage is fed out via pin 13 and R4 to pin 9, to pull the oscillator to a frequency which is a precise multiple of the input frequency.

4.94 The link on the divider IC3 can be set for division either by 5 or by 10. In the 9919 is should be set in the LK1 position, for division by 5, thus giving a multiplication factor of 50 to the input signal. This is equivalent to multiplication by 100 because the signal does not pass through the ÷ 2 stage IC9 (Fig.4) of the normal 'B' channel signal path.

CHAPTER 5

MAINTENANCE

TABLE 4: TEST EQUIPMENT REQUIRED

Item	Description	Remarks
1	Digital Multimeter Racal 9077	Provides 10 mV resolution on 50V range. DC input resistance 10MΩ
2	Oscilloscope	Bandwidth d.c. to 50 MHz Sensistivity 50 mV/cm
3	Frequency Standard	1 MHz; accuracy ±1 part in 10^8 Output 1V r.m.s. nominal
4	VHF Signal Generator Racal 9061/9062/9064 or HP.8640	Required range 15Hz - 550MHz Output 5mV - 1V r.m.s. into 50Ω Signal-to noise ratio better than 40 dB
5	UHF Signal Generator H.P. 612	Required range 500 - 1100MHz Output 5mV- 1V r.m.s. into 50Ω
6	RF Millivoltmeter Racal 9301A	Required frequency range: 10kHz to 530MHz. Measurement: 1 mV to 3V
7	Coaxial leads, 50Ω (quantity 2)	BNC to BNC. Length 3ft. (1 metre) approximately.
8	Terminating Pad, BNC 50Ω (quantity 1)	
9	Terminating connector, BNC. 50Ω (T Piece, quantity 1)	
10	Power Supply, a.c. single phase, line neutral and earth. Stability ± 2%	Supply voltage must be within an appropriate range. See page Tech. Spec. (5)

REMOVAL OF COVERS

5.1 Removal of the top cover is necessary in order to change the voltage tapping on the mains transformer.

WARNING: DANGEROUS AC VOLTAGES ARE EXPOSED WHEN COVERS ARE REMOVED WITH AC SUPPLY CONNECTED.

(1) Set the POWER switch to 'off', switch the a.c. supply at the supply point and unplug the power lead.

(2) Remove 4 screws from the top and bottom covers.

(3) Remove the rubber plugs (located near to the rear end) from both side panels of the instrument and slacken, by about two turns, the screws revealed.

(4) Grip the rear panel assembly and ease it back from the main case to the maximum extent available (about 5 mm).

(5) The rear edge of either cover can now be lifted and the cover withdrawn outwards and rearwards.

(6) To replace the covers reverse the above procedure.

TRANSFORMER VOLTAGE SELECTION

5.2 The instrument will normally be dispatched with the transformer primary tapping set to the 223-251V supply range. To check the selection proceed as follows.

(1) Unplug the power cable from the supply and remove the top cover (see previous paragraph).

(2) Refer to the diagrams on the next page:-

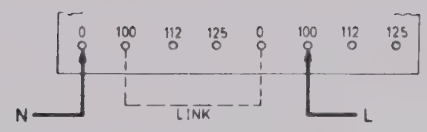
(a) Note the diagram which corresponds to the local a.c. supply voltage.

(b) Connect the correct link(s) and make the required line lead connection (L) as indicated in the appropriate diagram.

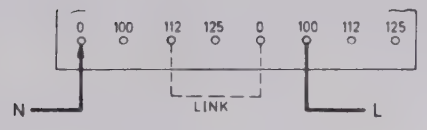
(3) Verify that the label on the rear panel indicates correctly the selected voltage range. Alternative labels are provided with the instrument for ranges other than 223-251V.

(4) Replace the top cover.

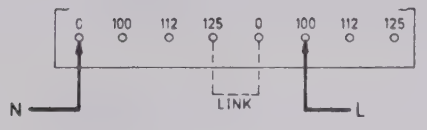
188-212V



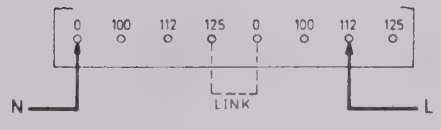
200-225V



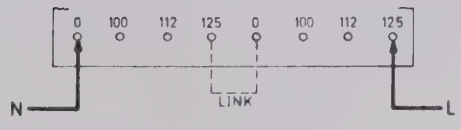
212-239V



223-251V

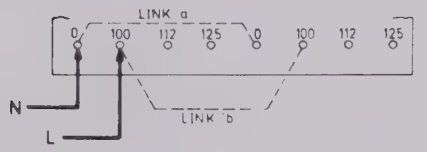


235-265V

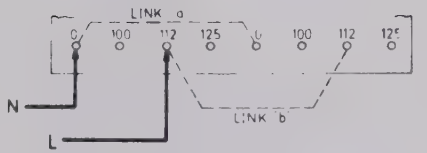


188V TO 265V

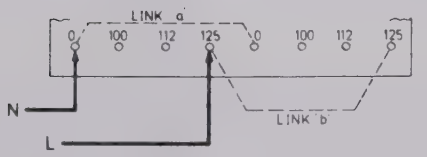
94-106V



106-119V



118-132V



94V TO 132V

Mains Transformer Voltage Selection Diagrams

Fig. 5·1

FUSES

5.3 (1) Check that the power fuse on the rear panel is correctly rated for the supply voltage, as follows. The fuse is a glass cartridge type, 5 x 20 mm.

Supply Range	Fuse Rating	Racal Part No.
188V - 265V	125 mA anti-surge	23-0043
94V - 132V	250 mA anti-surge	23-0031

POWER LEAD

5.4 Fit a suitable plug to the power lead in accordance with the standard colour code:-

Brown ..... Line
Blue ..... Neutral
Green/Yellow ..... Earth

POWER SUPPLY CHECK

5.5 (1) Remove the top cover and prepare the power supply as described in the preceding paragraphs.

(2) Set the rear panel switch to MAINS.

(3) With power supply connected, switch POWER to ON.

(4) Using the multimeter (Page 5.1, Table 1, item 1) check the d.c. voltages at the following points on the main p.c.b. (relative to chassis). Figure 3 at the back of the book shows the component layout. There are no adjustments in the d.c. power supply circuit.

Circuit Diagram	Test Point	Measurement
Fig. 5	Pin 14 (collector Q50)	+5.1V ± 0.15V
Fig. 5	Pin 8 (collector Q52)	-4.9V ± 0.25V
Fig. 5	CDI Chip pin 24	+2.2V ± 0.2 V
Fig. 4	Junction L5 and C42	+24V ± 2.4 V

NOTE: There are no adjustments in the power supply circuit. If the 5V supplies are outside the limits given above, the mains supply voltage and the transformer line lead connection and links (see page 5-3) should be carefully checked. If these are correct the zener reference diode D29 should be checked.

STANDBY CHECK

5.6 (1) Switch to STANDBY

(2) Press the CHECK/OPERATE RESET switch to RESET, and release.

(3) Check that the display is on and that the OVERFLOW/STANDBY indicator is extinguished.

(4) Verify that after approximately $1\frac{1}{2}$ minutes the display extinguishes and the OVERFLOW/STANDBY indicator illuminates.

(5) Repeat operation (2) and check that the display comes on.

PERFORMANCE TESTS AND CALIBRATION

NOTE: If the Racal Synthesized Signal Generator is used, with its frequency standard synchronised to that of the 9919, a readout accuracy of ±1 count will be obtained.

Segment, Decimal Point and Self Check.

5.6 (1) Set the rear panel switch to MAINS or BATTERY, according to power supply.

(2) Connect the a.c. supply (if used).

(3) Set the POWER switch to ON. If using the battery power, verify that the BATTERY LOW indicator is not illuminated. (Illumination indicates that batteries need charging).

(4) Set the following controls:-

(a) INPUT switch to'A'.
(b) CHECK/OPERATE/RESET switch to CHECK.
(c) NORMAL/BURST switch to NORMAL.

(5) Verify an 'all eights' display with satisfactory segments, and decimal point (d.p.) positions, as in Table 5.

TABLE 5

Segment Check

Resolution Switch Setting	Display	Units Indication
1 kHz	88888.888	MHz
100 Hz	8888.8888	MHz
10 Hz	888.88888	MHz
1 Hz	88888.888	kHz

(6) Set the INPUT switch to 'B' and verify a 1 MHz count in accordance with Table 6 below. Check that the GATE/CHARGING indicator, and the appropriate units indicator, are illuminated.

TABLE 6

SELF CHECK READOUT

Resolution Switch Setting	Display (±1 count)	Units Indication
0.1 Hz	1000.0000	kHz
1 Hz	01.000000	MHz
10 Hz	001.00000	MHz
100 Hz	0001.0000	MHz

(7) Set the CHECK/OPERATE/RESET switch to OPERATE and the INPUT SWITCH TO LF.

(8) Verify a display of 000000.01 (±5 counts) in all positions of the RESOLUTION switch. Check that the GATE/CHARGING indicator and Hz indicator are illuminated.

Sensitivity/Burst/AGC Check: Input 'B'

5.7 Test Equipment — Page 5-1 Table 4

(1)	VHF Signal Generator	Item 4
(2)	Oscilloscope	Item 2
(3)	BNC Terminating Connector and 50Ω load.	

5.8 Procedure

(1) Set the controls as follows:-

(a) INPUT switch to 'B'
(b) CHECK/OPERATE/RESET switch to OPERATE.
(c) NORMAL/BURST switch to NORMAL
(d) RESOLUTION switch to 10Hz position

(2) Terminate the 'B' input socket into 50Ω and apply a 100 MHz signal at 10mV r.m.s.

(3) Adjust R50 on the main p.c.b. (if necessary) for a stable display of the input frequency.

(4) Gradually reduce the input signal level, while adjusting R50 to maintain a stable display, until the most sensitive setting is found.

(5) Refer to the tests in Table 7. At each frequency reduce the input level to zero, then slowly increase it until the threshold level for a stable display is reached. Verify that such levels are not higher than those in the Table.

(6) Change the input frequency to 10MHz and monitor, with an oscilloscope the a.g.c. voltage at pin 12 of IC35. (see IC35a on circuit Fig. 4).

(7) Slowly increase the input signal level from zero to approximately 100 mV r.m.s. and verify that the a.g.c. voltage follows in a positive direction, changing from 0V to 1.1V ± 0.1V.

(8) Disconnect the input signal. Set the MODE switch to BURST and the RESOLUTION switch to 10Hz position.

(9) Press the CHECK/OPERATE/RESET switch to RESET and release. Check that the display is extinguished but that the decimal point remains visible.

TABLE 7

'B' Input Sensitivity Check

Resolution Switch	Applied Frequency	Input level for correct counting not to exceed:-
0.1Hz	20Hz	8mV
1Hz	1kHz	8mV
10Hz	10kHz	8mV
10Hz	20MHz	8mV
10Hz	30MHz	8mV
10Hz	80MHz	8mV
10Hz	105MHz	40mV

(10) Set the signal generator to 105MHz at 500mV r.m.s. Reconnect to the 'B' input socket while observing the display which should first show'all zeros' then go to a reading of the input frequency, which is held after a single gate time.

(11) Again select RESET and verify that the same reading is obtained.

Sensitivity and AGC Check: Input 'A'

5.9 Test Equipment — Page 5-1 Table 4

(1)	VHF Signal Generator	Item 4
(2)	UHF Signal Generator	Item 5
(3)	RF Millivoltmeter	Item 6
(4)	Multimeter	Item 1
(5)	BNC 'T' Piece	

Procedure

5.10 (1) Set the controls as follows:-

(a) INPUT switch to 'A'

(b) CHECK/OPERATE/RESET switch to OPERATE
(c) MODE switch to NORMAL
(d) RESOLUTION switch to 100Hz position

(2) Connect a 1 GHz signal at 100mV r.m.s. to the 'A' input socket

(3) Set R71 on the main p.c.b. to the mid-position (see circuit diagram Fig. 4) and verify a correct frequency display.

(4) Set the RESOLUTION switch to 10Hz position and check that the OVERFLOW/STANDBY indicator illuminates.

(5) Disconnect the input signal.

(6) Set the RESOLUTION switch to 100Hz position and set R71 fully clockwise.

(7) Set the signal generator to 500MHz. Connect to the 'A' input using a BNC 'T' piece.

(8) Using an r.f. millivoltmeter, adjust the input signal to 7.4mV.

(9) Adjust R71 anticlockwise until the unit just starts to count correctly.

(10) Apply the frequencies listed in Table 8. In each case set the input level below 7.4mV then increase slowly to find the level at which correct counting commences. Verify that up to 1GHz counting starts cleanly, with no tendency to lose or gain counts.

TABLE 8

Sensitivity Check: Input 'A'

Input Frequency	Input level for correct counting not to exceed:-
1.12GHz	40mV
1 GHz	8mV
800 MHz	8mV
500 MHz	8mV
250 MHz	8mV
75 MHz	8mV

(11) Press the CHECK/OPERATE/RESET switch to RESET and release. Check that the display resets to zero.

(12) With 75MHz applied, vary the input signal level from zero to 100mV, at the same time monitor the a.g.c. voltage change at the rear panel AGC output pins, using a multimeter. Verify that the a.g.c. voltage follows the input in a positive direction with a change from +1V ± 0.2V to +5V ± 0.2V.

(12) Disconnect the multimeter and millivoltmeter.

Burst Check: Input 'A'

5.11 Test Equipment — Page 5-1 Table 4

VHF Signal Generator — Item 4

5.12 Procedure

(1) Apply a signal of 1GHz at 500mV to the 'A' input socket.

(2) Set the controls as follows:-

(a) INPUT switch to 'A'
(b) MODE switch to BURST
(c) RESOLUTION switch to 100Hz position

(3) Disconnect the signal generator from the 'A' input socket.

(4) Press the CHECK/OPERATE/RESET switch to RESET and release. Verify that the display is extinguished but that the decimal point remains visible.

(5) Reconnect the input signal while observing the display, which should first display 'all zeros' then go to a reading of the input frequency, which is held after a single gate time.

(6) Again select RESET and verify that the same reading is obtained.

(7) Return the MODE switch to NORMAL and disconnect the signal generator.

Overload Indicator Check

5.13 This facility can be checked using a.u.h.f. generator capable of supplying up to 8.5V r.m.s. output at 100MHz, connected to the 'A' input. The OVERLOAD INDICATOR should illuminate at an input voltage in the range 5.5V to 8.5V r.m.s.

Battery Charging Checks

5.14 The charging current, with the optional battery pack fitted, will vary considerably during the 14 hour charge period. The approximate charging currents over the middle range of the charging period are as follows:-

Battery 'A' (+5V)

Trickle charge rate 80-90mA

Full charge rate..... .650-750mA

Battery 'B' (-5V)

Trickle charge rate..... 8-12mA

Full Charge rate..... 95-105mA

The above charge rates can be checked by measuring the voltage drop across the charge path resistor and calculating the current, as described in paras. 5.15 and 5.16.

Charge Rates Checks by Voltage Measurement

5.15 Battery 'A' (+5V)

(1) Remove both covers. Check that the battery pack is fitted (see para. 5.23) and the a.c. supply connected.

(2) Set the rear panel BATTERY/CHARGE/MAINS switch to CHARGE (for full rate charging) and the front panel POWER switch to ON.

(3) Set the multimeter to the 10V d.c. range.

(4) Connect the multimeter across the 3.9Ω , 2.5W resistor R138 (located in rear left hand corner).

CAUTION: Dangerous a.c. voltages are present in this area. Take great care when measuring across R138.

(5) Measure the voltage across the resistor; calculate the current and compare with the data in para. 5.14.

(6) Set the BATTERY/CHARGE/MAINS switch to MAINS (for trickle charge).

(7) Repeat operation (5)

5.16 Battery 'B' (-5V)

(8) Identify the 22Ω, ½W resistor R146 which is located at right angles to R73 and beneath the corner of the mains transformer tag board. Measure the voltage across this resistor; calculate the current and compare with the data in para.5.14

(9) Set the BATTERY/CHARGE/MAINS switch to CHARGE (for full rate charging).

(10) Repeat operation (8)

Internal Standard Output /External Standard Input Check

5.17 Test Equipment — Page 5-1 Table 4

(a)	External Frequency Standard, 1MHz.	Item 3
(b)	Oscilloscope	Item 2
(c)	BNC 'T' piece and coaxial leads BNC-BNC	

5.18 PROCEDURE

(1) Set the oscilloscope to 100ns/cm and connect to the 1MHz O/P socket on the 9919 rear panel (unterminated).

(2) Trigger the oscilloscope from the 1MHz external frequency standard, using a 'T' piece connector.

(3) Verify an approximately 1:4 rectangular output waveform at 1MHz, 3V p-p The trace will be moving slowly across the screen.

(4) Connect the external standard, via the 'T' piece, to the EXT STD I/P socket of the 9919, check that the oscilloscope trace locks and the EXTERNAL STANDARD indicator on the 9919 illuminates.

(5) Disconnect the test equipment.

FREQUENCY STANDARD CALIBRATION

5.19 The 'cycle drift' method of frequency calibration, described below, is suitable for oscillators which have temperature stability characteristics of up to 1 part in 10^8. For high stability oscillators, such as the Racal 9421 and 9442, the use of specialised equipment such as the Tracor Frequency Difference Meter Type 527A is recommended, if the optimum calibration is to be achieved.

5.20 Test Equipment:-

(1) Oscilloscope
(2) 1 MHz external frequency standard, with accuracy better than one part in 10^8.

5.21 Procedure

(1) Allow a suitable warm-up period (not less than one hour for a temperature-controlled oscillator).

(2) Set the oscilloscope time base to 1 μs/cm.

(3) Connect the 1 MHz external standard to the 'External Trigger' input of the oscilloscope.

(4) Connect the oscilloscope lead to the inner pin of the '1 MHz OUTPUT' socket on the rear panel (Screen to chassis).

(5) Observe the oscilloscope display and check that in a period of 10 seconds not more than one cycle of displayed waveform moves past a fixed point on the oscilloscope face. This corresponds to an accuracy of 1 part in 10^8.

(6) If necessary, adjust the mechanical tuning via the aperture in the rear panel to obtain a stationary trace. Frequency Standard 9421 has two trimmers, Coarse and Fine.

OPTIONAL LF MULTIPLIER CHECK

5.22 Set the INPUT switch to LF. Apply frequencies of 20 Hz and 6 kHz to the 'B' input socket at 8 mV r.m.s. Verify correct display from each frequency.

DISMANTLING

Removal of Display PCB

5.23 Complete removal of the Display PCB should be avoided if possible, because of the risk of damage to the plastic ribbon wiring loom when unsoldering it. All normal servicing and repair of the Display PCB can be done without complete removal. If the ribbon wiring has to be replaced the Part Number is 10-2538.

5.24 Removal Procedure

(1) Disconnect power supplies. Remove covers (para. 5.1).

(2) Remove the carrying handle as follows:-

(i) Insert a suitable tool such as a flat bladed screwdriver into the slot in the boss of each carrying handle and prise off the cap, thus exposing the retaining screws.

(ii)Extract the screws which hold the carrying handle to the main frame, and remove the handle.

(3) With the handle removed slide back the short length of coloured metal strip into the space normally occupied by the handle boss. This will allow access to the screws which secure the front panel to the main frame. Remove these screws.

(4) Remove the cap from the arm of the RESOLUTION switch.

(5) The front panel assembly can now be carefully withdrawn as far as the wiring permits.

(6) To detach the Display Assembly:-

(a) Unsolder the earth connection and input capacitor connection at the 'B' Input socket.

(b) Unsolder the remaining connections, noting the colour coding.

(c) Remove the four Pozidriv screws which secure the p.c.b. to the front panel. The p.c.b. can now be removed.

Removal of Main PCB

5.25 Due to excellent accessibility for servicing, removal of the main p.c.b. will rarely be necessary. It can be withdrawn either from the front or the rear. The rear panel method is described below.

(1) Completely remove the two screws which are referred to in cover removal (para. 5.1).

(2) Remove the covers and withdraw the rear panel as far as the wiring permits.

(3) Unsolder the wiring between rear panel items and main p.c.b.

(4) Unsolder the connections between the main p.c.b. and the regulator transistors on the side frame, and the rectifier on the rear panel.

NOTE: If preferred the transistors and rectifier can remain connected to the p.c.b. and be unscrewed from their mountings, but these items are not supplied with a replacement p.c.b.

(5) Cut the plastic strap which secures the large electrolytic capacitors, to the side frame. (Refer to para. 5.26 for the replacement of this strap).

(6) Remove the five Pozidriv screws which secure the p.c.b. to the main frame, and slide out the p.c.b. towards the rear.

Replacement of Main PCB

5.26 When re-fitting a main p.c.b. a new capacitor retaining strap should be fitted as follows:-

(1) Slide out the coloured metal strip from its slot on the outside of the left hand side frame.

(2) Thread the strap through the slots in the side member, then refit the metal strip.

(3) Fit and secure the main p.c.b.

(4) Fasten the capacitor strap.

(5) Refit the rear panel. Solder the connections, and secure the three regulator transistors to the side frame, and the bridge rectifier to the rear panel.

(6) Refit the two screws in the side members.

(7) Refit the covers when tests are completed. Replace the rubber plugs over the side panel screws.

FITTING BATTERY PACK OPTION

Battery Pack Kit

5.27 All items are contained in Battery Pack Option Kit, Part. No. 11-1251.

Fitting Instructions

5.28 (1) Switch off, disconnect the a.c. supply and remove the top cover

(2) Looking at the front of the instrument, screw the two mounting brackets to the threaded holes on the inner faces of the side members using the M4 screws and crinkle washers.

(3) Take the battery pack assembly, with batteries and the connecting lead to the left. Carefully lower the assembly onto the mounting brackets so that the slots line up with the screw holes in the brackets.

(4) Insert four M4 screws, with plain and crinkle washers, into the screw holes and make secure.

(5) Plug the connecting lead on to pins 43 to 46 on the main p.c.b. These pins are located in front of the Battery/Charge/Mains switch wafers and are spaced to prevent reversed connection.

(6) Replace the top cover. Check the instrument on battery power. Charge the batteries if necessary.

FITTING LF FREQUENCY MULTIPLIER ASSEMBLY (OPTION 09)

5.29 The LF Multiplier p.c.b. is attached by two screws to the right hand side panel of the instrument, towards the rear.

(1) Remove the top cover (para. 5.1).

(2) If the ovened frequency standard unit is fitted, it must be detached by removing the two retaining screws from the rear panel and moving the unit to one side. Do not unsolder the connections.

(3) Connect pins 1 to 5 of the LF Multiplier p.c.b. to the main p.c.b. in accordance with the circuit diagram (Fig. 5).

(4) Attach the LF Multiplier p.c.b. to the side panel using two M3 screws, and spacers, to the threaded holes provided. Dress the wiring neatly.

(5) Refit the frequency standard unit.

(6) Replace the top cover, then carry out an operational check.

FITTING OVENED FREQUENCY STANDARD UNIT

5.30 The following instructions are for fitting a fast-warm-up frequency standard unit in place of a discrete component oscillator p.c.b.

Procedure

5.31 (1) Unsolder the leads from pins 1, 2 and 3 of the discrete component oscillator p.c.b. Extract the two retaining screws (and spacers) from the rear panel and remove the p.c.b.

(2) Remove the black plate (if fitted) from the rear panel trimming aperture, and retain the screws.

(3) Attach the optional frequency standard unit to the inner face of the rear panel, align the fixing holes in the top of the unit with the rear panel holes and make secure with two M3, 6mm, screws. (The screws removed with the black plate can be used).

(4) Solder the connecting leads to pins 1, 4 and 7 of the frequency standard base, as shown in the circuit diagram.

(5) If frequency standard Type 9421 is being fitted, check that pins 5 and 6 on the base are linked.

(6) Carry out the instrument CHECK procedure to verify satisfactory functioning.

(7) Calibration of the frequency standard must be carried out before operational use. Refer to para. 5.19.

(8) Replace the instrument cover.

SECTION 3

PARTS LISTS

CIRCUIT DIAGRAMS

AND

COMPONENT LAYOUTS

ORDERING OF SPARE PARTS

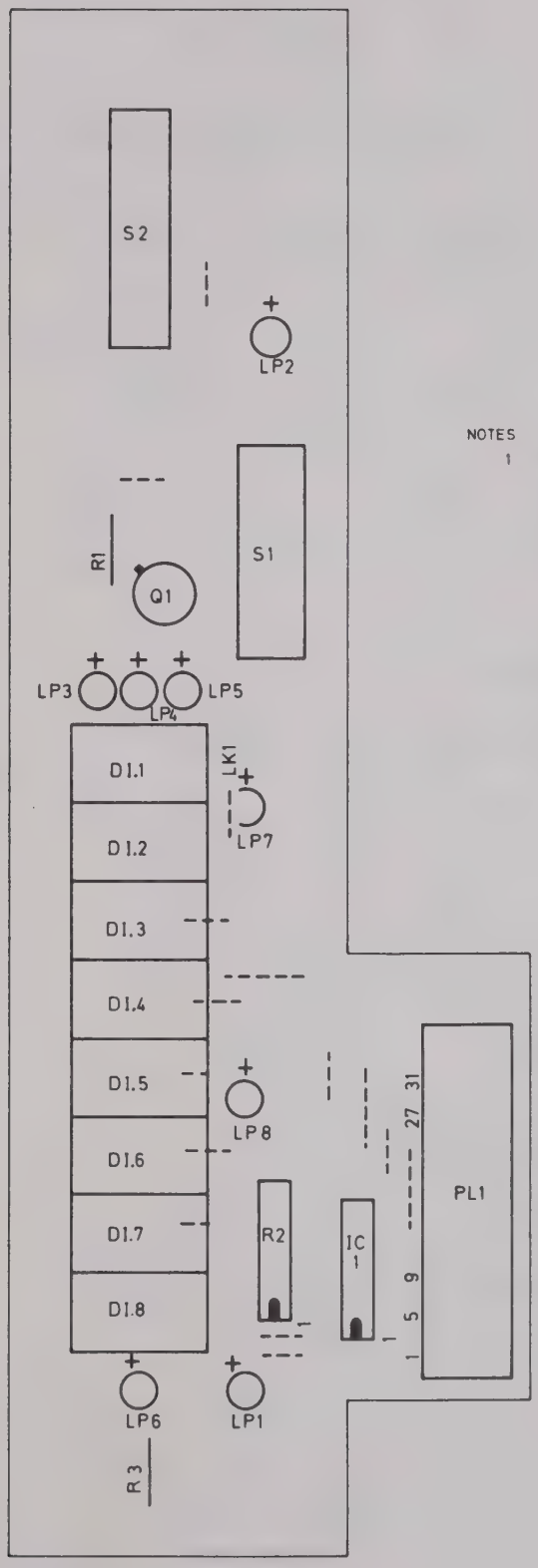
1. To be assured of satisfactory service when ordering replacement parts the customer is requested to include the following information.

   (a) Instrument type and serial number.

   (b) The type reference of the Assembly in which the particular item is located (for example, '19-0834').

   (c) The Racal Part number and circuit reference of each item being ordered.

   It should be noted that a minimum charge of £5 sterling is applicable to all U.K. orders.



NOTES

1 COMPONENTS ARE PREFIXED '1' ON CIRCUIT DIAGRAMS FIG 4 AND FIG 5

WOH 8005 19-0853
1

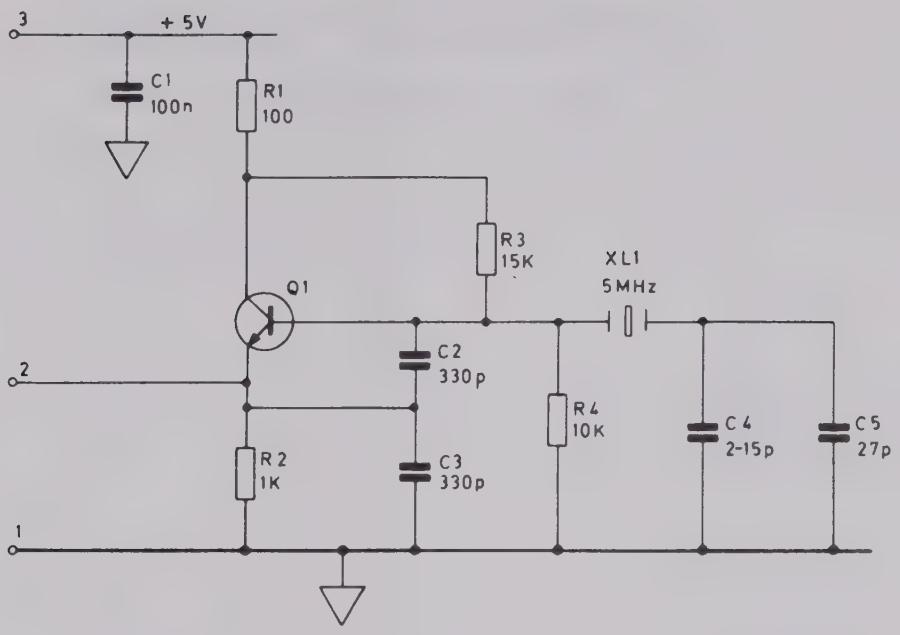
Component Layout: Display Assembly 19-0853 Fig.1

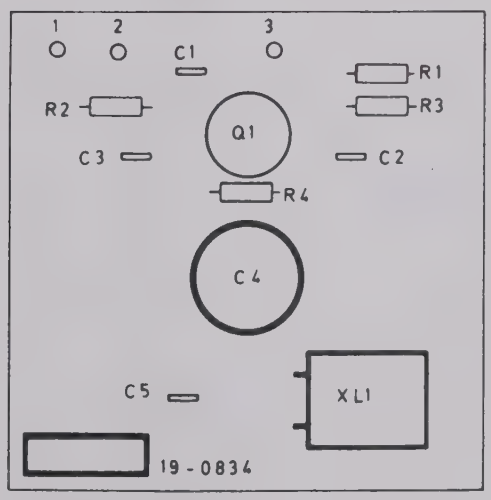
PARTS LIST

DISPLAY ASSEMBLY 19-0853

NOTE: These component references are prefixed '1' on the circuit diagrams (Figs 4 and 5).

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
20-2331	Carbon Film	¼	5	330	R1
20-5506	Resistor Array			47	R2
20-2471	Carbon Film	¼	5	470	R3
	Semiconductors				
22-4128	BCD/7 Segment Decoder/Driver (SN74247)				IC1
22-6079	Transistor npn			(ZTX313L)	Q1
	Switches				
23-4088	Slide switch 2-way (MODE)				S1
23-4080	Slide switch 3-way (INPUT)				S2
	Indicators				
26-1505	Digital Indicator, 7 segment				DI1-DI8
26-5004	Indicator lamps, LED (red)				LP1-LP8
	Connector				
10-2538	Connector Assembly				





WOH 8005	19-0834
1	

Circuit And Layout:
5MHz Oscillator PCB 19-0834

Fig.2

PARTS LIST FOR FIG.2

5MHz CRYSTAL OSCILLATOR ASSEMBLY (19-0834)

(Frequency Standard Option 04C)

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
20-2101	Carbon Film	$\frac{1}{4}$	5	100	R1
20-2102	Carbon Film	$\frac{1}{4}$	5	1k	R2
20-2103	Carbon Film	$\frac{1}{4}$	5	10k	R4
20-2153	Carbon Film	$\frac{1}{4}$	5	15k	R3
	Capacitors	V		F	
21-1616	Ceramic	12	20	100n	C1
21-2621	Silver Mica	125	5	27p	C5
21-2631	Silver Mica	125	5	330p	C2,3
21-6030	Trimmer			2-15p	C4
	Transistors				
22-6017	Silicon NPN (2N2369)				Q1
	Crystal				
17-2087	Crystal Assembly, 5MHz				XL1

PARTS LIST

CHASSIS, FRONT AND REAR PANELS (Figs. 4 and 5)

Part No.	Description	Rat.	Tol %	Value	Component Reference
CHASSIS ASSEMBLY COMPONENTS (11-1159)					
	Capacitors	V		F	
21-0575	Electrolytic	16		4700µ	C100
21-0576	Electrolytic	25		2200µ	C101
21-4528	Polyester	400	10	47n	C102
	Transistors				
22-6117	(MJE 370)				Q50
22-6081	(MJE 520)				Q51, Q52
FRONT PANEL COMPONENTS (11-1164)					
	Switches and Sockets				
23-4044	Switch Toggle, CHECK/OPERATE/RESET				S50
23-4064	Switch Toggle, POWER				S51
23-3204	Socket, BNC, chassis				SK50
23-3030	Socket, BNC, bulkhead				SK51
REAR PANEL ASSEMBLY COMPONENTS (11-1165)					
17-4049	Transformer, mains				T50
22-1650	Bridge rectifier, 200V, 2A (VS248)				D50
23-0043	Fuselink (118V/265V) 125 mA antisurge				FS50
23-0031	Fuselink (94V/132V) 250 mA antisurge				FS50
23-0044	Fuseholder for FS50				
23-3005	Socket BNC. STD input and output				SK52, 53
23-3194	Power Input (Mains) plug and filter				PL50
	Frequency Standard options 04A and 04B, see Tech. Spec.				
19-0834	Frequency Standard PCB option 04C, see Parts List 2.				

PARTS LIST FOR FIG.4 AND FIG.5

MAIN PCB ASSEMBLY 19-0852

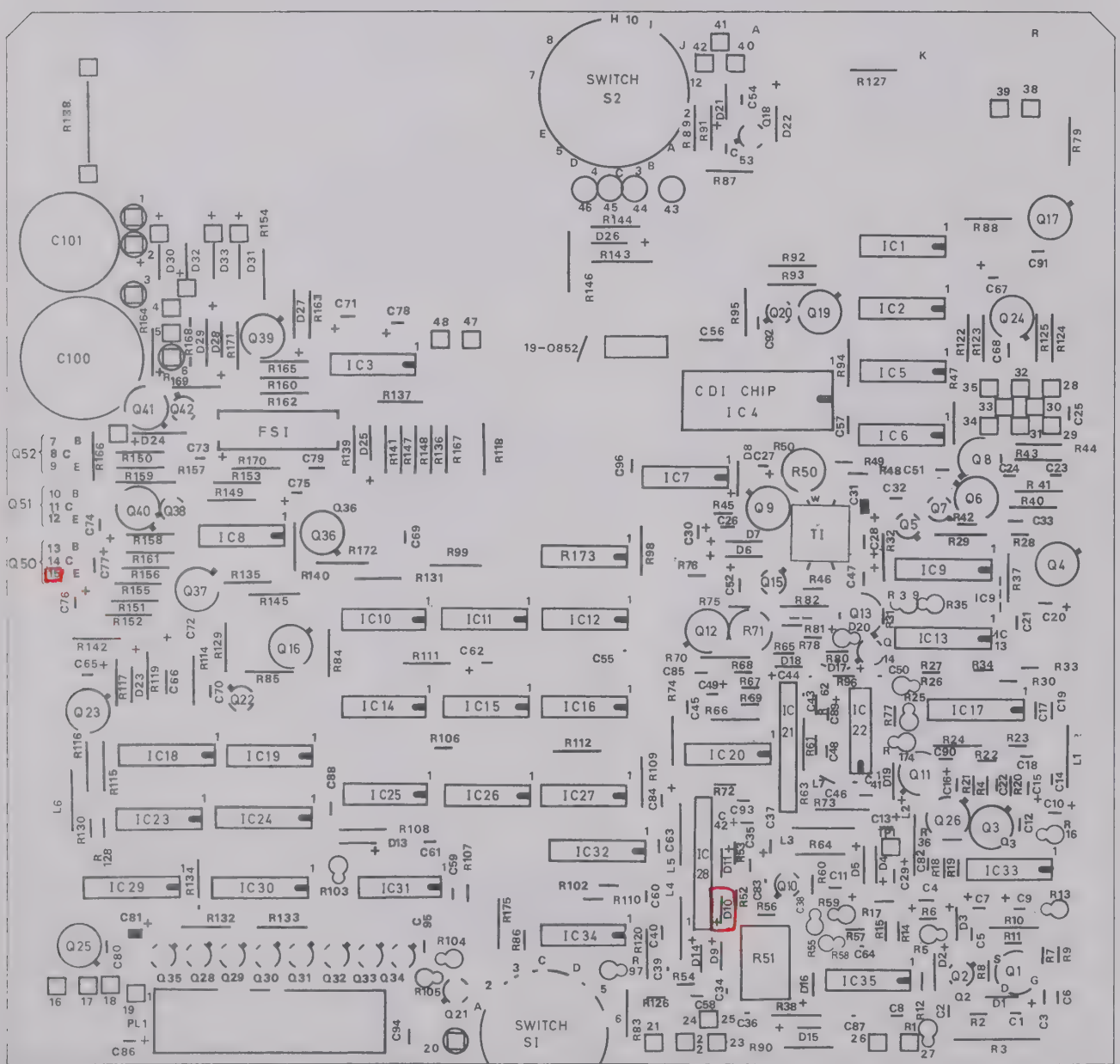
Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
20-1514	Carbon Film	0.1	5	100	R68,78,96
20-1515	Carbon Film	0.1	5	180	R42,48
20-1516	Carbon Film	0.1	5	220	R20,107
20-1519	Carbon Film	0.1	5	68	R45,49, 54, 61
20-1522	Carbon Film	0.1	5	12	R7,9
20-1523	Carbon Film	0.1	5	120	R11
20-1526	Carbon Film	0.1	5	22	R81
20-1528	Carbon Film	0.1	5	2.2k	R12,23,60,67
20-1529	Carbon Film	0.1	5	33	R62,
20-1531	Carbon Film	0.1	5	47	R19
20-1532	Carbon Film	0.1	5	470	R4,52
20-1533	Carbon Film	0.1	5	5.6k	R128
20-1535	Carbon Film	0.1	5	820	R18
20-1536	Carbon Film	0.1	5	560	R27,30,80
20-1538	Carbon Film	0.1	5	10k	R17,21,75,76, 86,106,110,126, Rx
20-1539	Carbon Film	0.1	5	33k	R46
20-1540	Carbon Film	0.1	5	27	R69
20-1542	Carbon Film	0.1	5	4.7k	R14,28,130
20-1544	Carbon Film	0.1	5	1.2k	R22,31,53
20-1545	Carbon Film	0.1	5	1.5k	R6
20-1547	Carbon Film	0.1	5	2.7k	R77
20-2392	Carbon Film	¼	5	3.9k	R58
20-1549	Carbon Film	0.1	5	6.8k	R56
20-1551	Carbon Film	0.1	5	100k	R15,57,72,102
20-1554	Carbon Film	0.1	5	680	R33,34
20-1555	Carbon Film	0.1	5	15k	R65
20-1561	Carbon Film	0.1	5	1M	R2
20-2001	Carbon Film	¼	5	1.2	R37
20-2002	Carbon Film	¼	5	1.5	R164
20-2101	Carbon Film	¼	5	100	R38,47,129,135
20-2102	Carbon Film	¼	5	1k	R82,83,98,120 122,125,136,162
20-2103	Carbon Film	¼	5	10k	R73,79,84,88,94, 95,99,104,105,111, 123,133,137,140, 168,169,175
20-2105	Carbon Film	¼	10	1M	R55
20-2106	Carbon Film	¼	10	10M	R59
20-2122	Carbon Film	¼	5	1.2k	R119
20-2150	Carbon Film	¼	5	15	R92,93
20-2151	Carbon Film	¼	5	150	R131,166
20-2153	Carbon Film	¼	5	15k	R171
20-2155	Carbon Film	¼	5	1.5M	R141
20-2181	Carbon Film	¼	5	180	R118,174
20-2182	Carbon Film	¼	5	1.8k	R13,16,155
20-2183	Carbon Film	¼	5	18k	R103,108
20-2220	Carbon Film	¼	5	22	R152,161
20-2221	Carbon Film	¼	5	220	R44,144,167
20-2222	Carbon Film	¼	5	2.2k	R115,158
20-2223	Carbon Film	¼	5	22k	R66,116,134
20-2272	Carbon Film	¼	5	2.7k	R32,124
20-2331	Carbon Film	¼	5	330	R5, 64, 70, 89, 90 151,172
20-2332	Carbon Film	¼	5	3.3k	R43,147
20-2390	Carbon Film	¼	5	39	R41
20-2391	Carbon Film	¼	5	390	R63
20-2470	Carbon Film	¼	5	47	R1
20-2471	Carbon Film	¼	5	470	R157
20-2472	Carbon Film	¼	5	4.7k	R74,91,112,127, 145,156
20-1517	Carbon Film	0.1	5	330	R36
20-2473	Carbon Film	¼	5	47k	R29,165
20-2474	Carbon Film	¼	5	470k	R109
20-2560	Carbon Film	¼	5	56	R132
20-2561	Carbon Film	¼	5	560	R24,25,26,87 142,154
20-2562	Carbon Film	¼	5	5.6k	R85,97,114,117, 139,170
20-2681	Carbon Film	¼	5	680	R10,35,39,40,160
20-2682	Carbon Film	¼	5	6.8k	R148
20-3220	Metal Oxide	½	5	22	R146
20-3270	Metal Oxide	½	5	27	R143
20-3470	Metal Oxide	½	5	47	R159
20-4049	Metal Oxide	¼	1	3.9k	R163
20-4094	Metal Oxide	¼	1	6.8k	R150
20-4103	Metal Oxide	¼	1	1.2k	R153
20-4107	Metal Oxide	¼	1	5.6k	R149
20-4658	Metal Oxide	1	5	100k	R3
20-5055	WireWound	2½	5	3.9	R138
20-5750	Chip Resistor	3	1	70	R51
20-5503	Resistor Array			10k	R173
20-7025	Variable, Cermet			200	R50
20-7034	Variable, Cermet			2.2k	R72
	Capacitors	V		F	
21-1000	Tantalum	35	20	3.3µ	C13
21-1002	Tantalum	20	20	10µ	C7,9,11,16,62
21-1006	Tantalum	35	20	4.7µ	C42,84
21-1029	Tantalum	35	20	1.5µ	C26
21-1038	Tantalum	6.3	20	47µ	C4,10,15,20,27, 28,29,31,37,47, 49,52,67,71,72, 73,74,75,76,77, 78,81,86,89
21-1041	Tantalum	35	20	1µ	C65
21-1511	Ceramic	500	10	18p	C22
21-1513	Ceramic	500	10	27p	C90, 93,
21-1514	Ceramic	500	10	33p	C5
21-1516	Ceramic	500	10	47p	C1
21-1518	Ceramic	500	10	68p	C24
21-1532	Ceramic	500	20	1n	C54,55,68,69,79, 92
21-1545	Ceramic	25	-20+80	10n	C83
21-1547	Ceramic	18	-20+50	33n	C30
21-1548	Ceramic	10	-25+80	47n	C82
21-1589	Ceramic	10	-25+80	220n	C56,61,66
21-1609	Ceramic	100	-20+80	1n	C48
21-1610	Ceramic	100	-20+80	10n	C39,50,64,87, Cx
21-1616	Ceramic	12	-20+80	100n	C2,3,6,8,14,17, 18,19,21,23,25,32, 33,35,40,45,46,51, 53,57,58,59,60,63, 70,80,85,88,91,94 95,96
21-1626	Ceramic Chip				C34,36,44
21-1677	Ceramic			5.6p	C43
21-1680	Ceramic			10p	C41
21-1729	Ceramic	200	-20+80	10n	C38

Part No.	Description	Value	Component Reference
	Diodes		
22-0007	Germanium, gold bonded (D07)		D13
22-1029	Silicon (1N4149)		D1,2,3,4,5,6,7, 8,19,21,22,23,25, 26,28
22-1033	Silicon, Hot carrier (HP5082-2811)		D17,18
22-1058	PIN Diode (5082-3379)		D9,10,11,14
22-1068	Silicon Hot Carrier (HP5082-2800)		D15,16
22-1602	Silicon, rectifier, 100V, 0.5A, (IN4002)		D24,30,31,32, 33
22-1801	Voltage regulator 2.7V (BZX-83C-2V7)		D20
22-1807	Voltage regulator 4.7V (BZY 88-C4V7)		D27
22-1854	Voltage regulator 5.1V (BZY 88-C5V1)		D29
	Integrated Circuits		
22-4045	Quad 2 input nor (7402)		IC10
22-4060	Quad 2 input nand gate (7403)		IC16
22-4061	Open collector hex inverter (7405)		IC34
22-4124	Schottky 3 input nand gate (74S10N)		IC6
22-4202	Dual Freq. comp.op. amp. (747)		IC3,8,20,35
22-4204	Hybrid VHF amp (OM335)		IC21
22-4216	Transistor array (CA.3083)		IC29,30
22-4217	Hybrid VHF amp. (OM320)		IC28
22-4221*	Differential video amp (72733) * Texas only		IC33
22-4507	Dual D-flip flop (10131L)		IC9
22-4514	Quad 2 input nor (10102)		IC13
22-4516	Schottky dual D-type Bistable (74S74)		IC12
22-4528	Line receiver (10116)		IC17
22-4530	Quad 2 to 1 Multiplexer (74LS157)		IC18
22-4531	Quad 2 i/p nand Schottky TTL (74LS00)		IC5,7,11,25
22-4532	Quad 2 i/p nor Schottky TTL (74LS02)		IC1,15,
22-4533	Hex invertor Schottky (74LS04)		IC14,27
22-4534	Dual D Bistable Schottky (74LS74)		IC26
22-4536	Decade counter (74LS90)		IC2
22-4538	VHF divide by 10 (SP8667B)		IC22
22-4546	O/C pos nand gate (74LS03N)		IC19,23
22-4557	3 input nand gate (74LS10)		IC31
22-4600	60MHz CD1 LS1 (Racal)		IC4
22-4706	Binary/BCD decoder (CMOS) (HEF4017P)		IC24
22-4707	Dual Retrig.M.Stable (CMOS) (MC14528CP)		IC32

Part No.	Description	Value	Component Reference
	Transistors		
22-6009	Silicon, npn, (2N4124)		Q17,22,41
22-6010	Silicon, pnp, (2N4126)		Q3
22-6079	Silicon, npn, (ZTX313L)		Q2,5,8,10,12,15, 16,18,20,21,23, 24,25,36,37,42
22-6101	FET, N channel (W300A)		Q1
22-6110	Silicon, pnp, (BFX48)		Q6,7,26
22-6113	Silicon, pnp, (ZTX550)		Q4,11,13,14,19 28,29,30,31,32,33, 34,35,38,39,40
22-6129	Silicon, npn, (BFX34)		Q9
	Inductors		
23-7018	RF choke, sub-miniature	47µH	L1,L2
23-7014	RF choke, sub-miniature	10µH	L3,L4,L6
23-7016	RF choke, sub-miniature	22µH	L5
17-3068	Inductor to Racal Drg.		L7
17-3214	Transformer, mains		T1
	Miscellaneous		
17-0085	Switch, lever, rotary		S1
17-0084	Switch, lever, rotary		S2
23-0006	Fuselink, quick action	1A	FS1
23-0034	Fuseholders		
23-3213	IC Holder 24 pin		

AMENDMENT INFORMATION

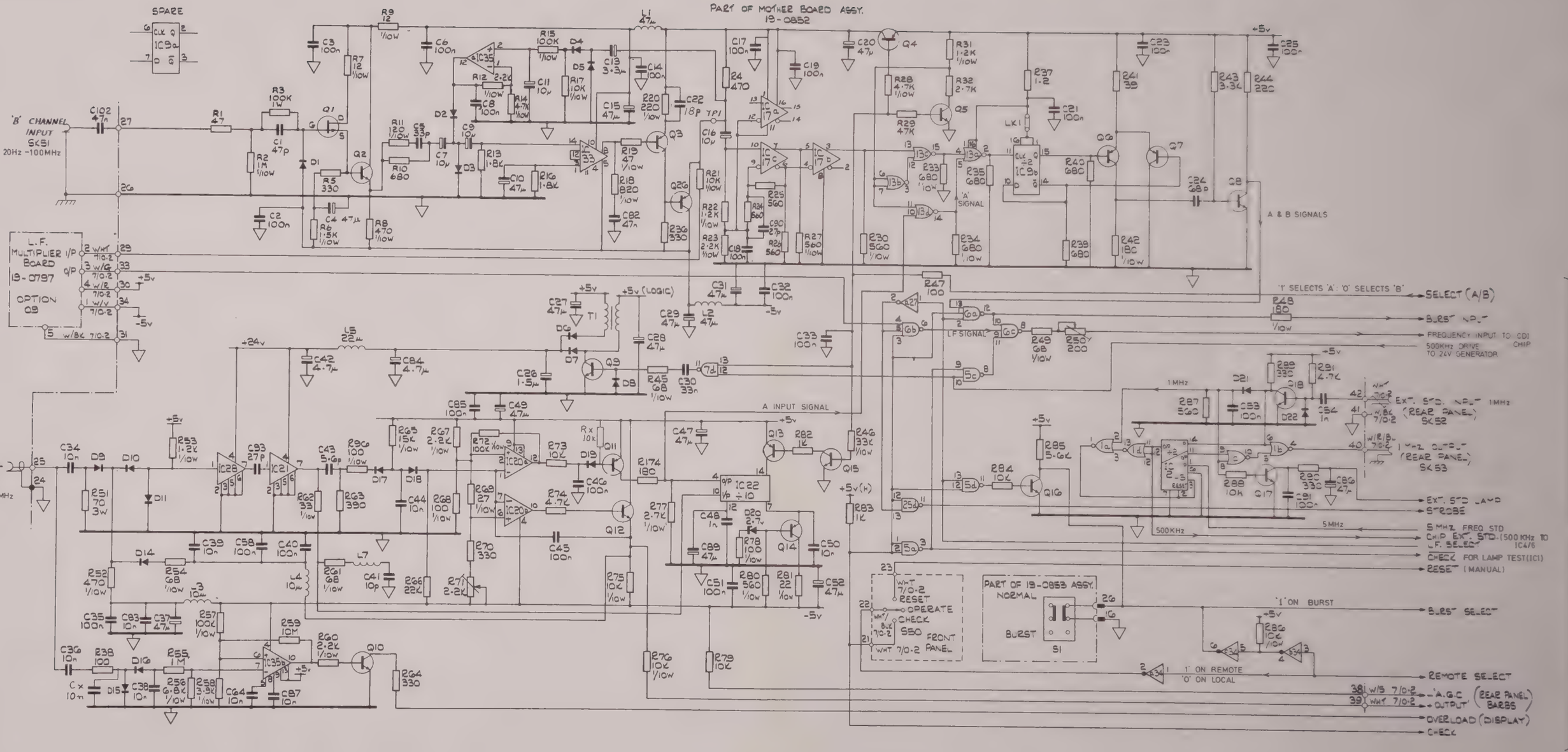
Check with Section 4 at the back of the book for latest information



NOTE: THE ASSOCIATED CIRCUIT IS SHOWN IN FIG.4 AND FIG.5

WOH 1005 19-0852

Component Layout: Main PCB Assembly 19-0852 Fig.3



INTEGRATED CIRCUIT DC CONNECTIONS		
IC REF	+5V PINS	0V PIN
IC 1, 5, 6, 7, 25, 27	14	7
IC 9, 13, 17	1 & 16	8
IC 2	5	10

RACAL

WOH 8005	9919 SHEET 2
1 2 3A	

Overall Circuit 9919 (Part 1) Fig. 4

PART OF MOTHER BOARD ASSY. 19-0852

CONTINUED ON FIG.4

BURST INPUT
SELECT (A/B)
CHECK

5 MHz
FREQUENCY INPUT
500 KHz

MAIN GATE
5 MHz

DATA OUTPUT

CDI CHIP IC4

EXT. STD.

HOLD /RESET

LATCH / UNLATCH

FRONT
BATT. CHARGE
MAINS
REAR
S2

MANUAL RESET FROM SWITCH S50
('1' = HOLD '0' NORMAL)

STROBE

RESOLUTION SWITCH S1
0·02S
0·2S
2S
20S

REMOTE SELECT
BURST SELECT
CHECK
EXT. STD. LAMP
OVERLOAD

L.F. SELECT

EXT. HOLD
HOLD/RESET
REMOTE SELECT
CHANNEL SELECT
DATA OUTPUT
OVERFLOW

PART OF DISPLAY ASSY. 19-0853

PART OF 19-0853 DISPLAY ASSY.

OVERFLOW/STANDBY

GATE CHARGE
BATT. LOW

POWER SUPPLY

+5v(H)

FREQ. STD
04A 9442
04B 9421
* LINK FITTED TO PINS 5 AND 6 OF BASE WITH 9421 ONLY

STD. BY OFF
S51
FRONT PANEL

TO SOLDER TAG ON TRANSFORMER FIXING

MAINS FILTER AND CONNECTOR

INTEGRATED CIRCUITS D.C. CONNECTIONS

IC REF	+5V PIN	0V PIN
5, 7, 10, 11 12, 14, 15, 16, 19, 23, 25, 26, 27, 31, 34.	14	7
IC 18, 24, 32	16	8

RACAL
WOH 8005 | 9919 SHEET 3
1 | 2 | 3

Overall Circuit 9919 (Part 2) Fig.5

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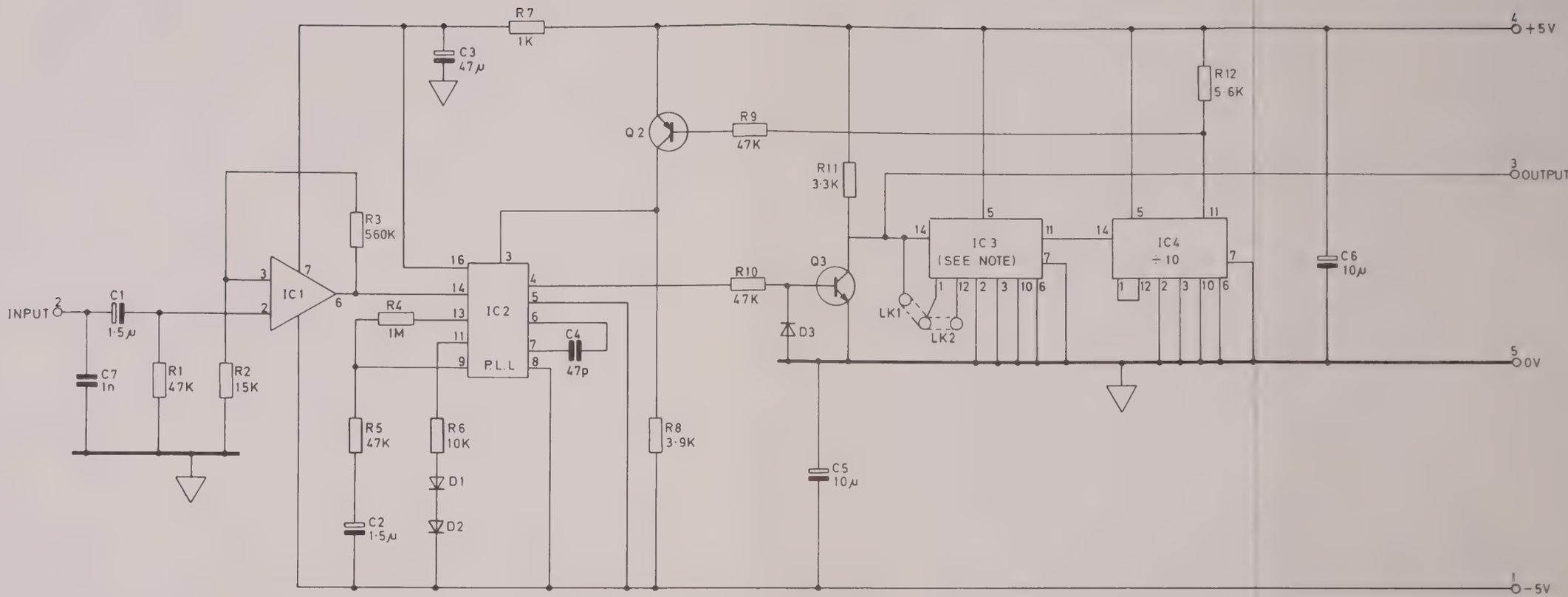
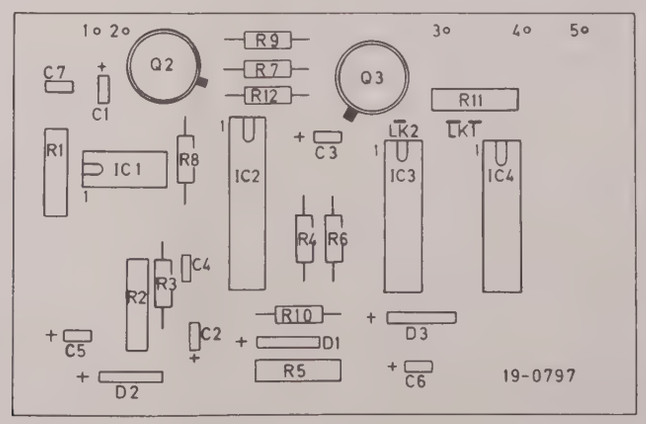
PARTS LIST

LF FREQUENCY MULTIPLIER ASSEMBLY 19-0797

NOTE: When fitting a new p.c.b. check that link is in the LK1 position.

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
20-2102	Carbon Film	¼	5	1k	R7
20-2103	Carbon Film	¼	5	10k	R6
20-2105	Carbon Film	¼	5	1M	R4
20-2153	Carbon Film	¼	5	15k	R2
20-2332	Carbon Film	¼	5	3.3k	R11
20-2392	Carbon Film	¼	5	3.9k	R8
20-2473	Carbon Film	¼	5	47k	R1,5,9,10
20-2562	Carbon Film	¼	5	5.6k	R12
20-2564	Carbon Film	¼	5	560k	R3
	Capacitors			F	
21-1002	Tantalum	20V	20	10µ	C5,6
21-1029	Tantalum	35V	20	1.5µ	C1,2
21-1038	Tantalum	6.3V	20	47µ	C3
21-1516	Ceramic	500V	10	47p	C4
21-1532	Ceramic	500V	20	1n	C7
	Diodes				
22-1029	Silicon (1N4149)				D1,2,3
	Integrated Circuits				
22-4111	Operational Amplifier (741C)				IC1
22-4536	Decade Counter, low power Schottky (74LS90)				IC3, IC4
22-4703	CMOS Phase-Locked Loop (CD4046AE)				IC2
	Transistors				
22-6017	Silicon NPN (2N2369)				Q3
22-6113	Silicon PNP (ZTX 550)				Q2





NOTE: FOR USE IN 9919 FIT LINK LK1.
DO NOT FIT LINK LK2.

WOH 8005	19-0797
1	

Circuit and Layout :
LF Multiplier Assembly

Fig.6

SECTION 4

APPENDICES

AND

CHANGE INFORMATION

OPTION 01

SERIAL TO PARALLEL INTERFACE UNIT

CONTENTS

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USING EQUIPMENT WHICH PROVIDES HOLD SIGNALS	3
Frequency Meters - Normal Use	4
Universal Counter Timers (UCT's)-Basic Hold Requirements	5
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UCT's Using Hold/Reset Mode	5
SPECIAL APPLICATIONS	5
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TABLES

Table 1 Flying Lead Connections
Table 2 50 way Connector

SERIAL TO PARALLEL INTERFACE UNIT

OPTION 01

INTRODUCTION

1. The interface comprises a metal box, measuring approximately 132 x 95 x 36mm containing the p.c.b: assembly 19-0851. Connections are made to printer or data display via a 50-way fixed socket and to the '99' instrument via a flying lead fitted with a 28-way edge connector. The unit is designed to operate with the following Racal counters, referred to in this description as the '99' series'

Frequency Meters	Universal Counter Timers (UCT)
9911	9901
9913	9903
9915	9905
9917	
9919	

2. Definition of Terms

(1) Hold Signal : a signal returned by the users equipment to the interface for control purposes.

(2) Print Command : a signal output by the interface to indicate that new measurement information is available.

(3) Print Hold input : An input which allows the user's Hold Signal to prevent the parallel information from changing.

(4) Hold/Reset input : An input which allows the user's signal to prevent the parallel information from changing and which resets the instrument when the Hold Signal returns to its normal state, thus starting a new measurement.

(5) Hold Control : An input to the interface which determines the mode of operation.

FUNCTION

3. The function of the Interface Unit is to convert the serial b.c.d. data output from a '99 series' counter to a static parallel form, suitable for driving a printer, data display or processing equipment.

4. The parallel output data is updated at the end of each gate time unless the printer (or other data processing equipment) is applying a Hold Signal. In addition to measurement data the interface also transfers information on decimal point position, selected range (gate time) and the 'overflow' state of the counter display. Information supplied is for 8 digits (excluding decimal point data) on all units except the 9917 which supplies information for 9 digits.

5. Fig. A1. shows the sequence of events which occurs at the end of the gate time. Note that when using counters 9911 and 9919 all timings are doubled, except the print command pulse width.

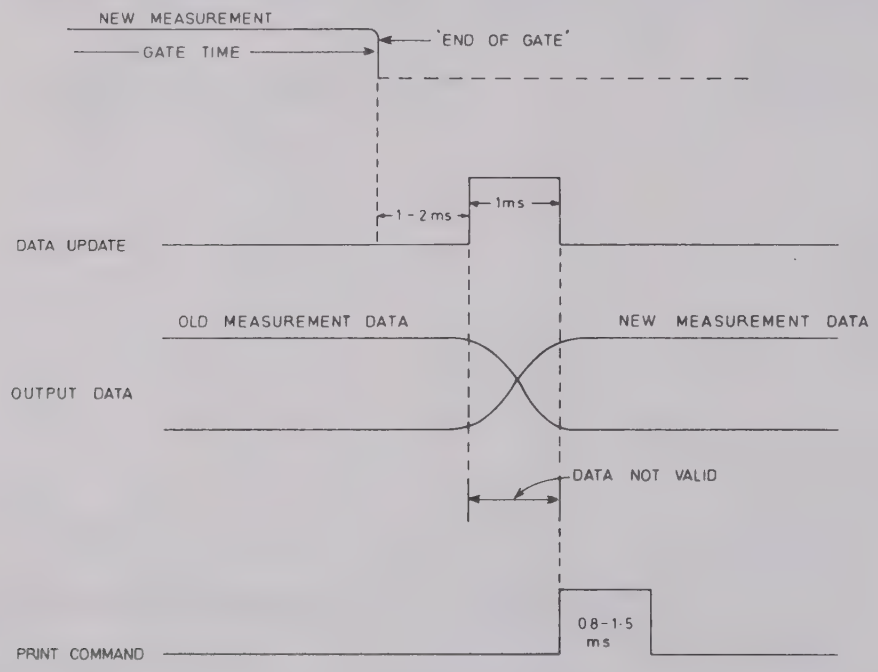


Fig. A1

CONNECTION

6. Before connecting the Interface Unit to the counter refer to the modes of operation in paras 8 to 18 and make the necessary changes to the 50-way connection or 28-way flying lead, according to the type of counter in use and the required function. All changes on the 50-way connection should be made at the customers connector.

7. Having checked the appropriate connection changes in paras 8 to 18, the interface should be connected up as follows:-

(1) Remove the black plate which covers the DATA OUTPUT aperture on the rear panel of the counter. Retain the two screws.

(2) Slacken off the cable clamp on the metal cover on the cable of the flying lead, and push the cover away from the connector.

(3) Plug the flying lead connector into the Data Output edge connector in the counter, noting the keyway which ensures correct orientation.

(4) To minimise r.f. radiation interference, the metal cover on the cables

(4) should be placed over the edge connector and held into place by the two screws which originally secured the cover plate removed in (1). The cable clamp should then be tightened.

(5) Connect the interface unit to the data processing equipment via the fixed 50-way socket.

MODES OF OPERATION

REMOTE DISPLAYS

Connections

8. If the interface is required to drive a remote display, or such other equipment that does not require the data to be held for a period longer than the gate time, check the following pin conditions on the 50-way connector:-

Pin No.	Required Connection
19	Must be either open circuit
24	or connected to OV.
49	

Latched Operation

9. The display is latched and is updated at the end of each gate time, irrespective of the counter function.

Unlatched Operation

10. (1) If the interface Unit is connected to a genuine remote display the subjective result is that the display will appear to follow the counter , for both latched and unlatched counter modes.

(2) The data outputs will be updated every 3 to 4 ms.

(3) The blue wire 'H' on the 28-way flying lead connector should be disconnected and reconnected to 'F' together with the violet wire. For other applications refer to paras 16 to 18.

USING EQUIPMENT WHICH PROVIDES HOLD SIGNALS

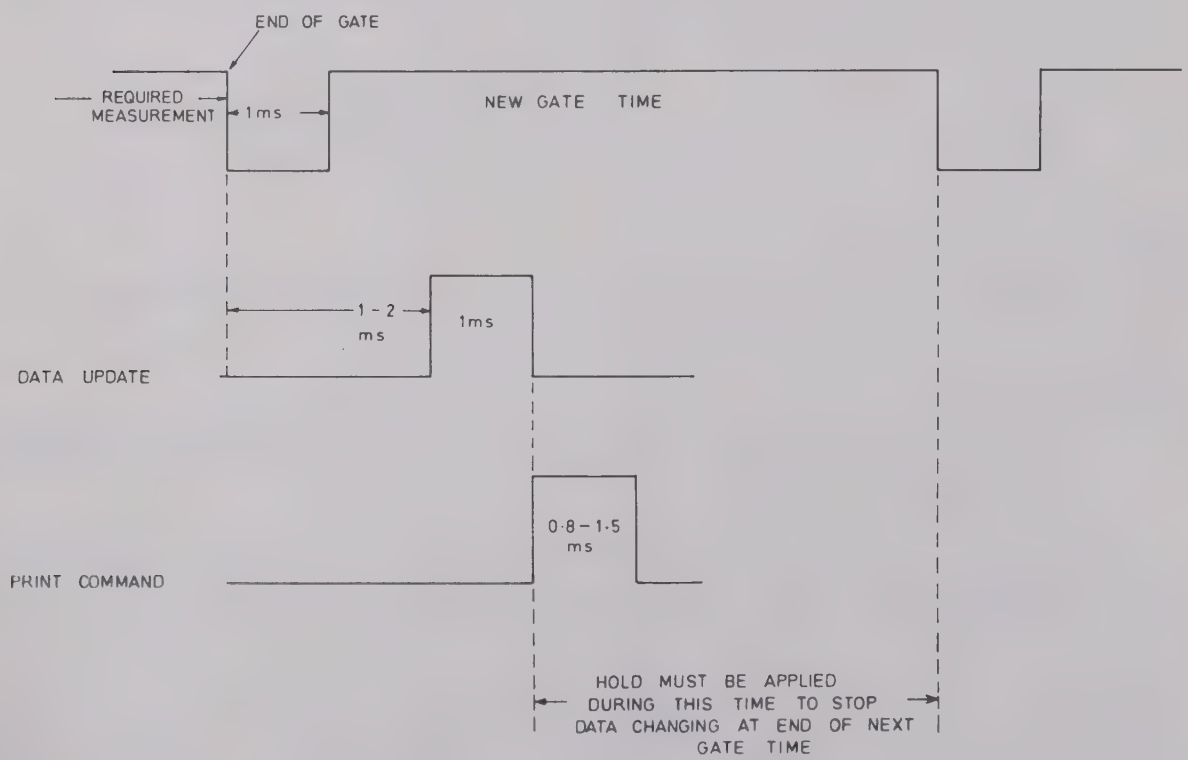
11. Differing instructions apply, depending on whether the counter is a frequency meter or universal counter timer (UCT) as described in paras 12 to 15.

Frequency Meters - Normal Use

12. (1) Check the following pin connections on the 50 way connector:-

Pin No.	Required Connection
19 and 24	Open Circuit, or connected to OV
49	Connected to the Hold signal

(2) The Hold signal (logic level '1' to hold) should be applied to the interface after receiving the Print Command signal, but before the end of the next gate time (ie 7 ms for 10 ms gate time), and should remain at logic level '1' for the period that the information on the data output is required to remain unchanged. Although the outputs from the interface will remain unchanged whilst a Hold is applied, the counter continues its normal measurement sequence, i.e. 'free run'. This has the advantage that the next Print Command will be given at the end of the gate time immediately following the release of the Print Hold. This result in a more rapid measurement sequence. From Fig. A2. it can be seen that a Print Command signal occurs 3 to 4 ms after an end of gate, by which time the gate time for a new measurement will have commenced. *


END OF GATE
REQUIRED MEASUREMENT
1 ms
NEW GATE TIME
1 - 2 ms
1ms
DATA UPDATE
0·8 – 1·5 ms
PRINT COMMAND
HOLD MUST BE APPLIED DURING THIS TIME TO STOP DATA CHANGING AT END OF NEXT GATE TIME

* NOTE: In the 9919 the timings are double those in Fig.A2

Fig. A2

Universal Counter Timers (UCT's) - Basic Hold Requirements

13. The measurement cycle of the 99 series of UCT's has two distinct phases; the Gate Time during which the measurement is made, and the Display Time during which the results are displayed. If the hold time required by the equipment to which the interface is connected is less than the display time, the remainder of the display time is effectively wasted. The interface can be used to shorten the display time, but in so doing the counter display is reset, which may not be convenient. For this reason the interface can be used with UCT's in two modes, the Print Hold and the Hold/Reset modes, as described in paras 14 and 15. It should be noted that, with UCT's, the interface will not produce a data change or Print Command signal from the operation of a front panel RESET control.

UCT's Using Print Hold Mode

14. In the Hold/Reset mode the Hold signal extends the display time indefinitely the next gate time commencing when the Hold is released or when the normal display period has ended, whichever period is the longer. The Hold signal must be applied within the display time period in order to halt the measurement cycle. The required pin connections on the 50 way connector are as follows:-

Pin No.	Required Connection
Pin 19	Connected to Pin 50 (or to 5V via 180Ω)
Pin 49	Connected to the Hold signal source
Pin 24	To be open circuit or connected to OV

UCT's Using Hold/Reset Mode

15. In the Hold/Reset mode the Hold signal (minimum width 5 ms) extends the display time indefinitely, but when it is released the counter display resets and a new measurement commences. This result in a more rapid measurement sequence, again the Hold signal must be applied within the display time period in order to halt the measurement cycle. The required pin connections on the 50-way connector are as follows:-

Pin No.	Required Connection
Pin 19	Connected to pin 50 (or to 5V via 180Ω)
Pin 24	Connected to the Hold signal source
Pin 49	To be open circuit or connected to OV

SPECIAL APPLICATIONS

Remote Display-Special Applications

16. When used in the unlatched mode with certain types of equipment other than remote displays (for example a digital comparator) there is a limit to the maximum possible counting rate. Therefore the reading for which the comparator is looking could be missed, i.e. there is a maximum update rate for the option of 3-4 ms. This corresponds to an input frequency of 200 Hz (N=1) on Totalize mode and a maximum resolution of 10ms on Time Interval mode. The counting rate can be increased if a degree of overshoot can be tolerated.

The maximum overshoot that will occur is given by:-

$$\text{Counting Rate} \times 4 \times 10^{-3} \text{ counts.}$$

It is advisable to use the Print Command as a 'data valid' signal in such systems.

Frequency Meters - Special Applications

17. In some applications it is not possible to use the interface in the manner described in Para 12. For example, in control systems, where the output of the interface is used as feedback to the device on the input of the counter, problems arise because the next gate time has already started before the information becomes available from the previous one. Therefore, even if the feedback correction is made almost instantly, the reading at the end of the next gate time will be incorrect. Alternatively, if the correction process takes more than one gate time, the end of gate time immediately following the process will also give incorrect results. These problems may be overcome by applying a Hold signal to the Print Hold input (pin 49) for the length of time that the correction takes, plus an additional time to ensure that the gate time from which the next data is to be taken cannot start until the correction process has been completed, as shown in Fig. A3.

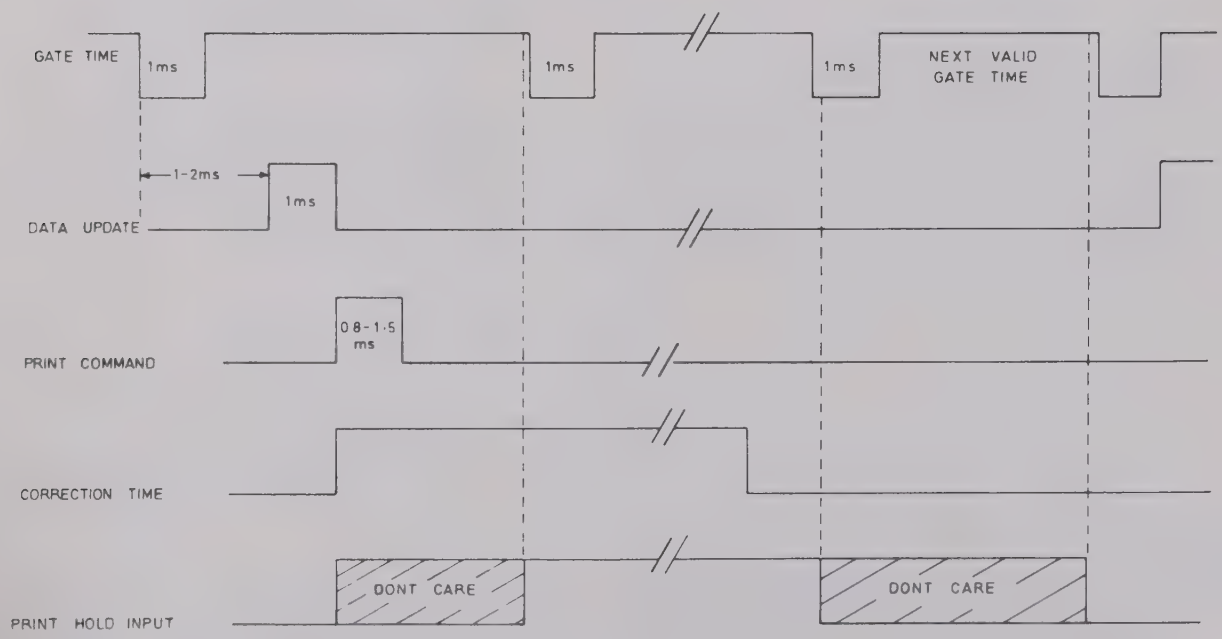


Fig. A3

18. An alternative to para 17, particularly when fast cycle times are desired, is to connect the Hold signal to the Hold/Reset input. If this is done, a stretched version must additionally be applied to the print Hold input (pin 49). The Hold signal should be at least as long as the correction process, and the signal applied to the Print Hold input should be approximately 200µs longer than that applied to the Hold/Reset input. This is to prevent the interface responding to the end of gate time produced by the reset. For cases where the correction time is short (less than the Print Command pulse width) this may be implemented by linking the Print Command output (pin 48) to the Hold/Reset input (pin 24) and by applying a stretched version of the Print Command to the Print Command to the Print Hold input (pin 49). In this way cycle times as short as 'Gate Time + 5ms' can be achieved. This is illustrated in Fig. A4.

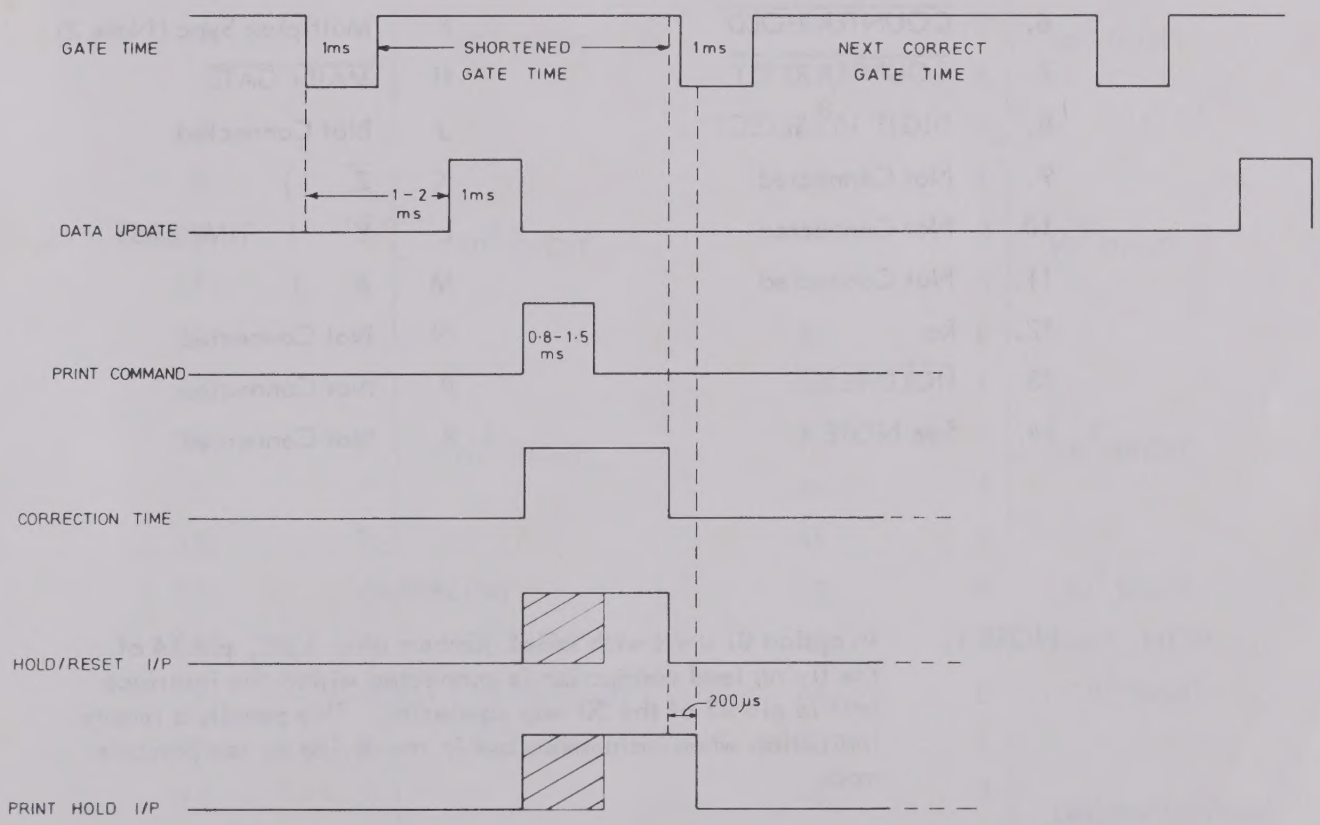


Fig. A4

TABLE 1.

FLYING LEAD CONNECTIONS

Pin No.		Pin No.	
1.	Not Connected	A	0V
2.	+ 5V (nominal)	B	$\overline{\text{OVERFLOW}}$
3.	KEYWAY	C	KEYWAY
4.	$\overline{4}$ BCD DATA	D	$\overline{1}$ BCD DATA
5.	$\overline{8}$	E	$\overline{2}$
6.	$\overline{\text{COUNTER HOLD}}$	F	Multiplex Sync (Note 2)
7.	$\overline{\text{COUNTER RESET}}$	H	$\overline{\text{MAIN GATE}}$
8.	DIGIT 10^8 SELECT	J	Not Connected
9.	Not Connected	K	$\overline{Z}$)
10.	Not Connected	L	$\overline{Y}$) TIME BASE
11.	Not Connected	M	$\overline{X}$)
12.	$\overline{Ro}$	N	Not Connected
13.	$\overline{\text{HOLD/RESET}}$	P	Not Connected
14.	See NOTE 1	R	Not Connected

NOTE 1. In option 01 units with serial numbers after 1389, pin 14 of the flying lead connection is connected within the interface unit to pin 43 of the 50 way connector. This permits a remote indication when instruments are in the divide by ten prescale mode.

NOTE 2. The multiplex sync. signal on pin F is 10 KHz, except with 9911 and 9919 instruments when it is 5 KHz.

TABLE 2.

50-WAY CONNECTOR

Pin No.	Facility		Pin No.	Facility	
1.	1	10^0 DIGIT	26.	1	10^1 DIGIT
2.	2		27.	2	
3.	4.		28.	4	
4.	8		29.	8	
5.	1	10^2 DIGIT	30.	1	10^3 DIGIT
6.	2		31.	2	
7.	4		32.	4	
8.	8		33.	8	
9.	1	10^4 DIGIT	34.	1	10^5 DIGIT
10.	2		35.	2	
11.	4		36.	4	
12.	8		37.	8	
13.	1	10^6 DIGIT	38.	1	10^7 DIGIT
14.	2		39.	2	
15.	4		40.	4	
16.	8		41.	8	
17.	OVERFLOW		42.	4	10^8 DIGIT
18.	1	10^8 DIGIT	43.	See table 1 NOTE 1.	
19.	HOLD CONTROL I/P		44.	8	10^8 DIGIT
20.	2	10^8 DIGIT	45.	1	DECIMAL POINT
21.	$\overline{X}$	TIME BASE	46.	2	
22.	$\overline{Y}$		47.	4	
23.	$\overline{Z}$		48.	PRINT COMMAND O/P	
24.	HOLD/RESET I/P		49.	PRINT HOLD I/P	
25.	0V		50.	+ 5V (VIA 180Ω)	